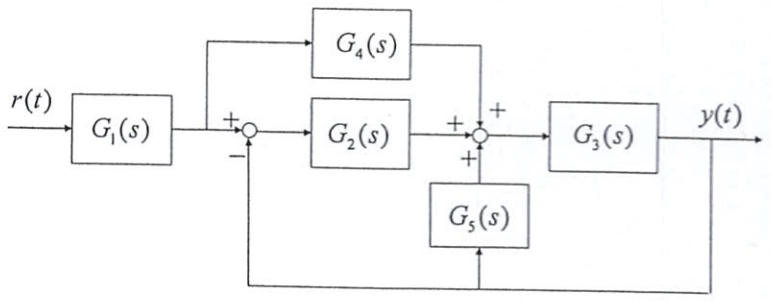
國立臺灣科技大學 107 學年度碩士班招生試題

系所組別：電機工程系碩士班丁二組

科　　目：控制系統與數位邏輯

Problem 1: (15 points) 說明：計算題 15 分

Consider the following system block diagram (SBD), use only three basic SBD operators: $\text{series}(G_1,G_2)\equiv G_1G_2$, $\text{parallel}(G_1,G_2)\equiv G_1+G_2$, and $\text{feedback}(G_1,\pm G_2)\equiv\frac{G_1}{1\mp G_1G_2}$, to find the system transform function $G(s)=\frac{Y(s)}{R(s)}$. **There is no point if you use other methods to solve this problem.**



Problem 2: (15 points) 說明：計算題 15 分

Draw the Bode plot of a negative unity-feedback system with loop transfer function $L(s)=\frac{10(s+10)}{s(s+1)(s+100)}$, and estimate the gain margin (GM) and phase margin (PM) from your Bode plot as accuracy as possible.

Problem 3: (15 points) 說明：計算題 15 分

Draw the root-locus plot (i.e. close-loop poles v.s. K) of a negative unity-feedback system with loop transfer function $L(s)=\frac{11s+6}{s(s+6)(s+K)}=0$, $K>0$, and determine the value of K such that the close-loop system has a pole at $s=-0.5$.

Problem 4: (5 points) 說明：設計題 5 分

Write an algorithm to implement a PI controller $\frac{U(s)}{E(s)}=P+\frac{I}{s}$, $P,I>0$, the input is the system error $e[n]=r[n]-y[n]$ and the output is the control input $u[n]$, where discrete-time signals $e[n]=e(nT)$, $r[n]=r(nT)$, $y[n]=y(nT)$ and $u[n]=u(nT)$, $n=0,1,2,\cdots$, and T is the sampling time.

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Problem 5: The four-bit universal shift register is shown in Fig. 1. Draw a block diagram of the IC with 16 pins, showing all inputs, outputs and two pins for the power supply. In addition, a function table for this IC is depicted. (12 points)

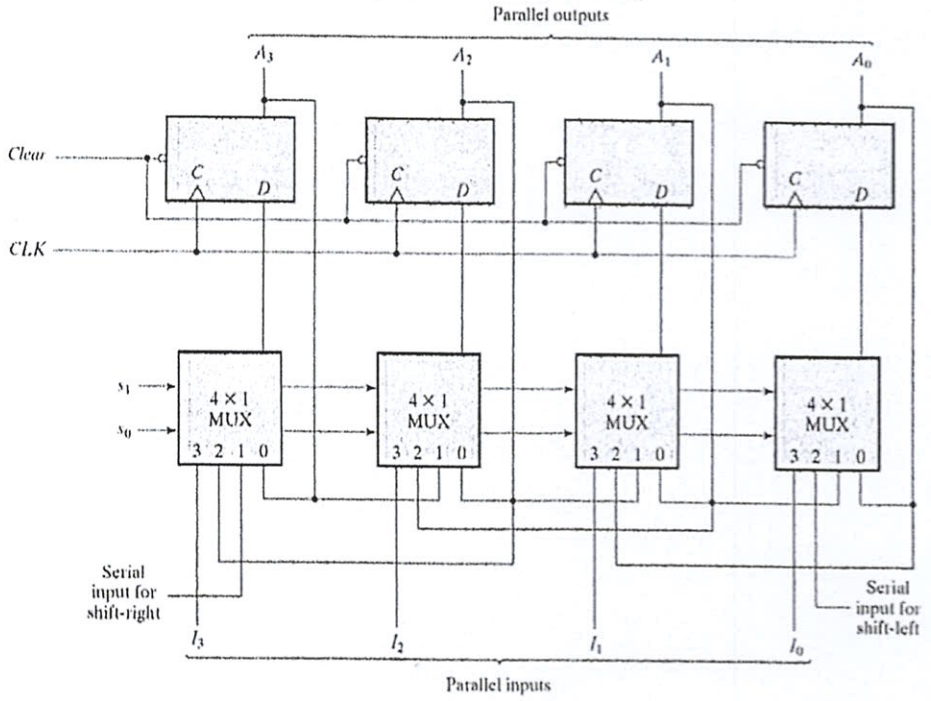
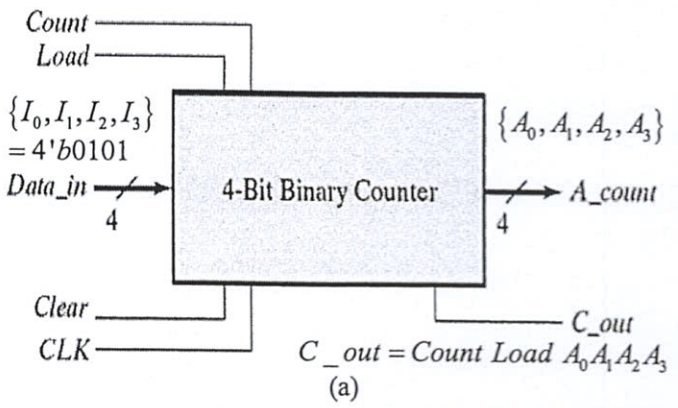


Fig. 1. Four-bit universal shift register.

Problem 6: Design a three-bit counter using T-FF such that the operation 000→111→110→101→100→ 011→010→001→000. The results must include state table, K-map, and logic diagram. (18 points)

Problem 7: Consider the 4-bit binary counter in Fig. 2. Given the following signals: (i) **initial begin** *CLK*=0; #5 forever *CLK*=~*CLK*; **end.** (ii) **initial fork** *Clear_b*=0; #20 *Clear_b*=1; **join.** (iii) **initial fork** *Count* =0; #50 *Count* = 1; #150 *Count* = 0; #200 *Count* = 1; **join.** (iv) **initial fork** *Load* =0; #250 *Load* = 1; #260 *Load* = 0; **join.** Plot and explain the responses including, *CLK, Clear_b, Count, Load,* $\{I_0, I_1, I_2, I_3\}$, $\{A_0, A_1, A_2, A_3\}$, and *C_out* for total 350ns. (20 points)



(a)

Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change

(b)

Fig. 2. Four-bit binary counter.