

國立臺灣科技大學 108 學年度碩士班招生試題

系所組別：資訊工程系碩士班

科目：資訊工程概論

(總分為 100 分)

1. In an operating system (OS), a *process* is a program in execution. (11%)
 - (a) A *process* may stay in one of five states. What are the five states? (5%)
 - (b) Which state will a *process* be moved to after it invoking a system call to request the OS to execute a **synchronous** I/O operation? (3%)
 - (c) Which state will a *process* be moved to after it invoking a system call to request the OS to execute an **asynchronous** I/O operation? (3%)

2. The basic algorithms for CPU scheduling include *First Come First Serve*, *Shortest Job First*, *Priority Scheduling*, and *Round Robin*. In addition, two more complicated scheduling algorithms are *Multi-Level Queues* and *Multi-Level Feedback Queues*. (11%)
 - (a) Which basic scheduling algorithm should we select if the average response time of a process is the major concern? (4%)
 - (b) Which basic scheduling algorithm is usually selected for scheduling a queue of CPU-bound processes within *Multi-Level Queues*? (3%)
 - (c) Among the six scheduling algorithms, which is able to distinguish between I/O-bound and CPU-bound processes? (4%)

3. Please answer the following questions. (11%)
 - (a) Suppose the variable, counter, is accessed concurrently by the two processes, PA and PB. If the value of counter is originally 6, what values may counter have after PA executes the statement, counter = counter + 1, and PB executes the statement, counter = counter - 2? (3%)
 - (b) When a dead lock occurs, four necessary conditions can be observed. What are the four necessary conditions? (4%)
 - (c) Three address-binding times are compile-time, load-time, and execution-time. In which binding time, will a logical address be different to its bound physical address? (4%)



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4. Given the graph in Fig. 1, please give the following representations of the graph. (10%)

(a) Adjacency matrix (5%)

(b) Adjacency list (5%)

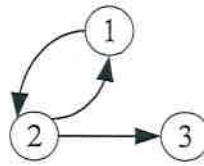


Fig. 1

5. Given the preorder and inorder sequences of a binary tree as follows: (15%)

Preorder: JIDHCBEFGA

Inorder: HDIBCJFEGA

Assume that each character represents a node in the tree.

(a) Please draw the corresponding binary tree. (10%)

(b) Please provide the postorder sequence of the tree. (5%)

6. Please show the minimum spanning tree of the graph in Fig. 2. (8%)

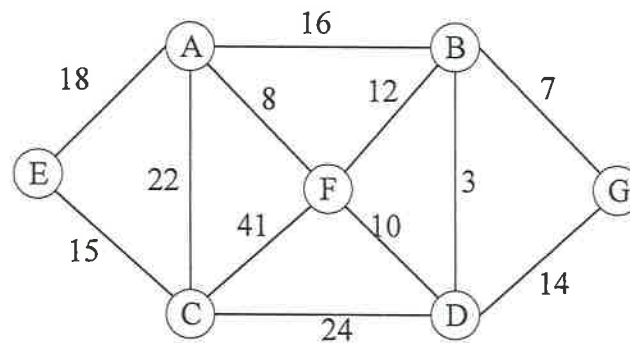


Fig. 2



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7. The table below shows the number of instructions and the CPI for each type of instruction in a program. Suppose the program is run on a computer with clock rate = 2 GHz. (14%)

Instruction Type	Instruction Count	CPI
A	2×10^9	1
B	3×10^9	2

- (a) What is the average CPI of this program? (4%)
- (b) Please determine the execution time for each type of instruction in this program. (4%)
- (c) Suppose we want the program to run **two times faster**. If **only one type** of instruction can be improved, how much should we improve the speed of Type A? How much should we improve the speed if Type B is improved instead? (6%)
8. For a five-stage (IF, ID, EX, MEM, WB) pipelined datapath with forwarding and consider the following MIPS instruction sequence with initial values of $\$t1 = 1$ and $\$t2 = 20$, please answer the following questions. (10%)
- ```
sw $t2, 20($s1)
add $t2, $t1, $t1
add $t2, $t2, $t2
lw $s3, 24($s1)
add $t3, $s3, $t2
```
- (a) Which register(s) is/are read in clock cycle 5? (3%)
- (b) What is the value of  $\$t2$  at the end of clock cycle 6? (3%)
- (c) How many clock cycles are required to finish the execution of this instruction sequence? (4%)
9. Suppose we have a processor with a base CPI of 1, assuming all references hit in the primary cache. Consider a two-level cache, where the miss rates per instruction at the primary cache and the secondary cache are 5% and 1%, respectively. Suppose the miss penalties for an access to the main memory and the secondary cache are 100 and 10 clock cycles, respectively. (10%)
- (a) What is the effective CPI for a one-level cache where **only the primary cache** is used without the secondary cache? (5%)
- (b) What is the effective CPI for a two-level cache where **both the primary cache and the secondary cache** are used? (5%)

