國立臺灣科技大學 110 學年度碩士班招生試題

系所組別：電機工程系碩士班丁二組

科　　目：控制系統與數位邏輯

(總分為 100 分)

Problem 1: system transfer function with initial conditions (10 points)

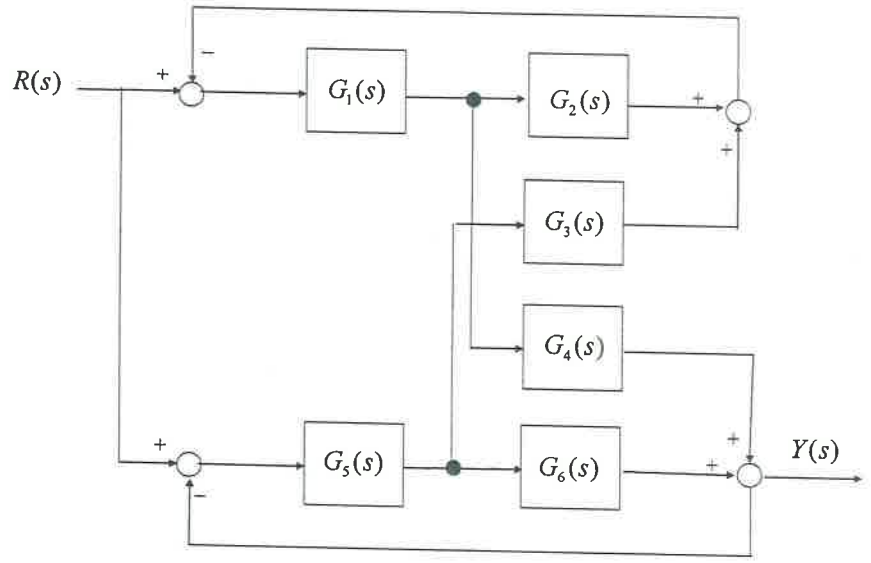
Given a linear system with system input-output transfer function $T(s)=\frac{Y(s)}{U(s)}=\frac{1}{s(s^2+1)}$; compute output $y(t), t\geq 0$ with initial conditions: $y(0)=1$, $\dot{y}(0)=-1$, $\ddot{y}(0)=0$, and zero input, $u(t)=0$, $t\geq 0$.

Problem 2: time and frequency responses (10 points)

Consider a control system with system transfer function $T(s)=\frac{Y(s)}{U(s)}=\frac{s+2}{s^2+2s+2}$; find frequency response bandwidth ω_{BW} and maximum overshoot $MO\%$ for unit-step response.

Problem 3: System block diagram (10 points)

Find the input-output transfer function $T(s)=Y(s)/R(s)$ of the system block diagram below.



Problem 4: Root-locus analysis (10 points)

Consider a negative unity-feedback system, $T(s)=\frac{L(s)}{1+L(s)}$, with loop transfer function $L(s)=\frac{8}{s(s+2)(s+K)}$; draw the root-locus of $T(s)$ for $0<K<\infty$. For higher score, the root-locus should be as detailed as possible.

Problem 5: Root-locus design (10 points)

Continue on Problem 4, design K such that the unit step response $y(t)$ of the closed-loop system, $T(s)$, having zero steady-state error $e_{ss}=\lim_{t\to\infty}(1-y(t))=0$, zero maximum overshoot $MO=0\%$ and 3dB bandwidth $\omega_{BW}\geq 0.5$ rad/sec.

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Problem 6 (10 points)

Find $F(x, y, z)$ in Fig. 1. You must present the details.

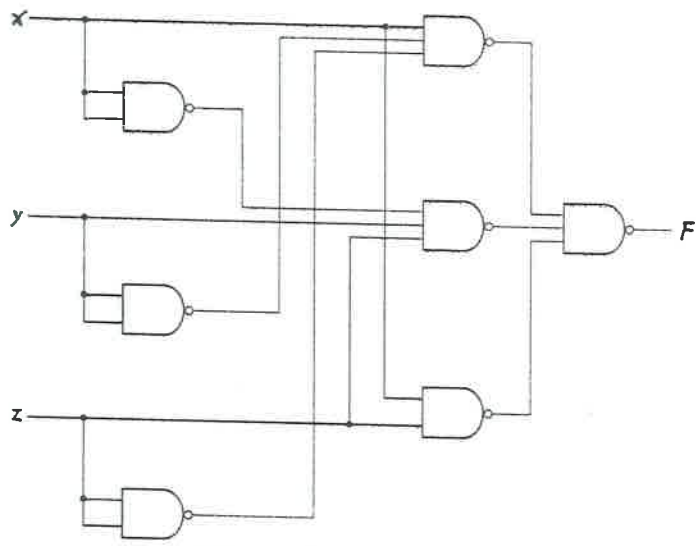

Fig. 1. Logic circuit.

Problem 7 (12 points)

Draw the state diagram of the machine described by the following Verilog HDL.

```
module Problem_6(output reg y_out, input x_in, clk, reset);
parameter s0=2'b00, s1=2'b01, s2=2'b10, s3=2'b11;
reg [1:0] state, next_state;
always@(posedge clk, negedge reset) //begin
if (reset==1'b0) state <=s0; else state <= next_state;
//end
always@(state, x_in) begin
y_out=0; next_state=0;
case (state)
s0: begin y_out=0; if (x_in) next_state=s1; else next_state=s0; end
s1: begin y_out=0; if (x_in) next_state=s2; else next_state=s1; end
s2: if (x_in)   begin y_out=0; next_state=s3; end else begin y_out=1; next_state=s2; end
s3: begin y_out=1; if (x_in) next_state=s0; else next_state=s1; end
default: next_state=s0;
endcase
end
endmodule
```

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Problem 8 (13 points)

In Fig. 2, a 4-bit binary counter with Load (L), Count (C), data input $I_i, i = 0,1,2,3$, Clear, CLK, and output $A_i, i = 0,1,2,3$ is presented. Its function table is in Table 1. How to use and some logic gates to count from 0 to 134, and then back to 0.

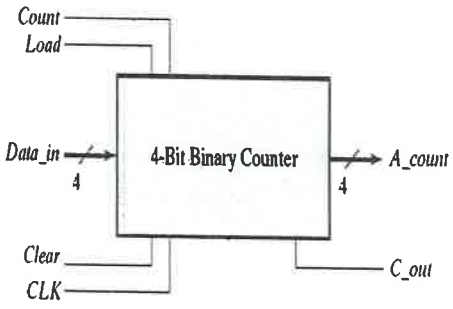

Fig. 2. 4-bit binary counter.

Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change

Table 1. Function table of 4-bit binary counter.

Problem 9 (15 points)

Consider the 4-bit (i.e., $A[3:0]$) up-down counter in Fig. 3. Given the following signals:

(i) **initial begin** *CLK*=1; #5 forever *CLK*=~*CLK*; **end.**

(ii) **initial fork** #10 *Reset_b=0*; #20 *Reset_b=1*; **join.**

(iii) **initial fork** *Down*=0; *Up* =0; #40 *UP=1; #150 Down=1; #200 UP=0; #250 Down=0*; **join.**

Plot and explain the responses including, *CLK, Reset_b, Down, Up*, and $A[3:0]$ for a total of 300ns. (Plot : 10 pts ; Explain : 5 pts)

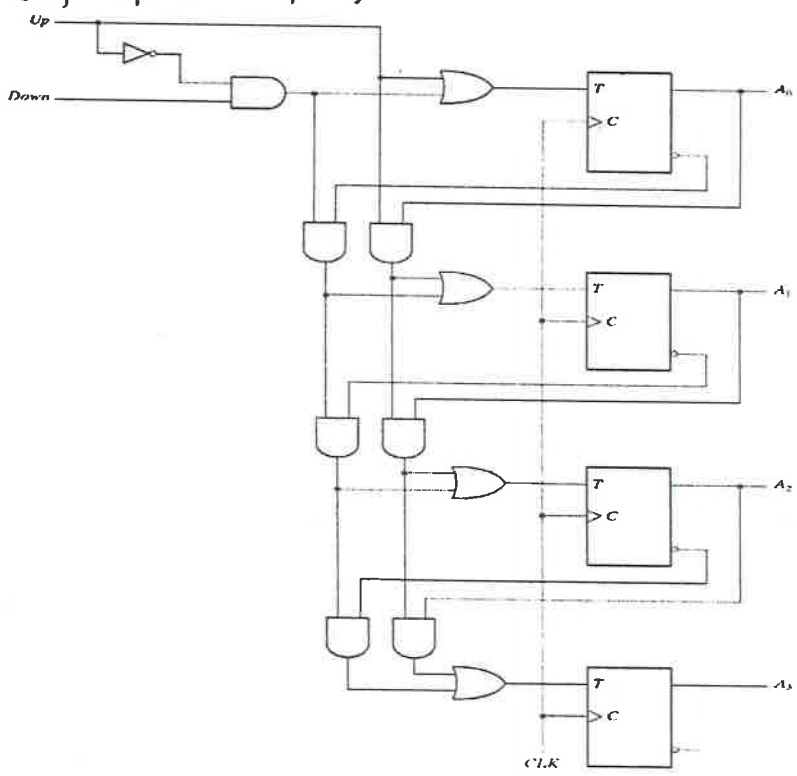

Fig. 3. 4-bit up-down counter.