

國立臺灣科技大學  
八十七學年度碩士班招生考試試題

所 別： 電機工程技術研究所  
學程別：

組別： 計算機組

科目： 計算機組織

1. Suppose the head of a moving-head disk with 200 tracks, numbered 0 to 199, is at track 53 initially. Consider an ordered disk queue with requests involving tracks 98, 183, 37, 122, 14, 124, 65, and 67.

What is the total head movement (tracks) needed to satisfy these requests for the following disk-scheduling algorithms?

- (a) First-Come, First-Served (8%)
- (b) Short-Seek-Time-First (8%)

2. Consider the control unit of Figure 1. Assume that the control memory is 32 bits wide (32 bits/word). The control portion of the micro-instruction format is divided into two fields. A micro-operation field of 15 bits specifies the micro-operations to be performed. An address selection field specifies a condition, based on the flags, that will cause a micro-instruction branch. The system has eight flags.

- (a) Determine the bit number in the address selection field and address field? (8%, 8%)
- (b) What is the size of control memory? (words) (8%)

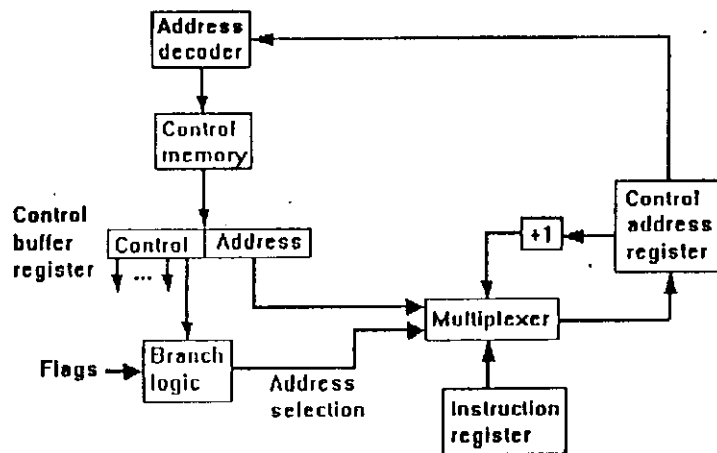


Figure 1

3. Plot and describe the architecture of memory system with the error correction capability. (10%)

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4. Table 1 shows three kinds of cables commonly used in the Ethernet physical layer implementation. Both RG-8U and RG-58U coaxial cables have a velocity factor of 0.66.
- What is the worst-case time interval between when a thicknet Ethernet station begins transmitting and when it detects a collision? (4%)
  - What is the physical length of a bit in the 10BASE-5 Ethernet? (4%)
  - How many bits may be on the cable simultaneously in thicknet Ethernet? (3%)
  - Suggest an average back-off time for this net after a collision. Justify your answer with a brief discussion. (3%)

Table 1 Ethernet Cabling

Cable	IEEE Standard	Maximum Cable Length (m)	Maximum Total Length (m)	Topology
RG-8U (thicknet)	10BASE-5	500	2,500	Bus
RG-58U (thinnet)	10BASE-2	185	1,000	Bus
Unshielded twisted pair (telephone wire)	10BASE-T	100	2,500 with thick back-bone	Star-bus (requires hub)

5. Consider the five-stage pipelined processor specified by the following reservation table:

	1	2	3	4	5	6
s1	X					X
s2		X			X	
s3			X			
s4				X		
s5		X				X

- List the set of forbidden latencies and the collision vector. (3%)
  - Draw a state transition diagram showing all possible initial sequences (cycles) without causing a collision in the pipeline. (3%)
  - List all the simple cycles from the state diagram. (3%)
  - Identify the greedy cycles among the simple cycles. (3%)
  - What is the minimum average latency (MAL) of this pipeline? (3%)
  - What is the minimum allowed constant cycle in using this pipeline? (2%)
  - What will be the maximum throughput of this pipeline? (2%)
  - What will be the throughput if the minimum constant cycle is used? (2%)
6. Explain the following terms related to shared-variable programming on multi-processors.
- Multiprogramming. (3%)
  - Multiprocessing in MIMD mode. (3%)
  - Multiprocessing in MPMD mode. (3%)
  - Multitasking. (3%)
  - Multithreading. (3%)