國立臺灣科技大學
八十七學年度碩士班招生考試試題

所　別：電子工程技術研究所　　組別：計算機組　　科目：計算機組織
學程別：

1. (10%) (DRAM)
A 16Mb DRAM chip has a word size $w = 8$ bits and has a 2-D organization with multiplexed row-column addressing.

   (a) If the column address is 10 bits, what is the size of the row address ?

   (b) How many copies of this DRAM are needed to make a $1G \times 32$-bit memory ?

2. (10%) (Register file design)
Using register-level components, design a three-port register file that contains four 16-bit registers. The symbol of this register file is shown in Figure 1.

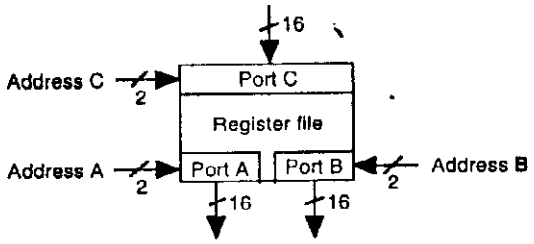

Figure 1: The symbol of a register file

3. (10%) (Pipelining)
Criticize the following statement:
"Increasing the depth of pipelining always increases performance."

4. (10%) (Precise interrupt)
Define the term *precise interrupt*. In what conditions an interrupt occurring during the execution of an instruction I is precise.

5. (10%) (Cache organizations)
Two system organizations for caches are (a) look-aside and (b) look through. Describe their pros and cons.

6. (10%) (DRAM types)
Currently, various fast access modes are supported in commercial DRAM chips. Among these the following ones are most important: fast-page mode, extended data output mode, synchronous DRAM, and rambus DRAM. Define informally these access modes.

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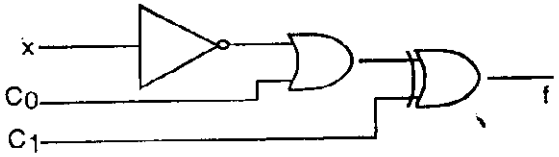
7. (20%) (ALU design)

(a) Consider Figure 2(a) and fill in the truth table in Figure 2(b).

(b) Using the circuit in (a) and a four-bit parallel adder, design a 4-bit arithmetic unit that can compute any of the following operations: $G = A$ (transfer A), $G = A + 1$ (increment A), $G = A + B$ (addition), $G = A + \overline{B} + 1$ (subtraction), and $G = A - 1$ (decrement A), where G, A, and B are the 4-bit output and the two inputs of the arithmetic unit, respectively.



(a)

C_1	C_0	f
0	0	
0	1	
1	0	
1	1	

(b)

Figure 2: ALU Design

8. (20%) (Two-way set-associative cache design)
A single 16K-byte two-way set-associative cache is used in a microprocessor. Each block (or line) of the cache contains 8 bytes and the microprocessor has address space of 2^{32} bytes.

(a) Assume that $1K \times 8$ SRAM chips are used for both cache Tag memory and cache data memory. How many SRAM chips are required for these two memories, respectively ?

(b) Using the SRAM chips in (a) and suitable TTL devices, design this cache memory. Ignore the block replacement and its related control circuits.