國立臺灣科技大學
八十八學年度碩士班招生考試試題

系所別：電機工程系碩士班　　組別：丙組　　科目：計算機組織

1. A computer consists of a CPU and an I/O device D connected to main memory M via a 1-word shared bus. The CPU can execute a maximum of 10^5 instructions per second. An average instruction requires five machine cycles, three of which use the memory bus. A memory read or write operation uses one machine cycle. Suppose that the CPU is continuously executing "background" programs that require 95% of its instruction execution rate but not any I/O instructions. Now the I/O device is to be used to transfer very large blocks of data to and from main memory M.
   (1) If programmed I/O is used and each 1-word I/O transfer requires the CPU to execute two instructions, estimate the maximum I/O data-transfer rate r_{MAX} possible through D. (10%)
   (2) Estimate r_{MAX} if DMA transfer is used. (If we assume that the DMA module can use all of machine cycles, and ignore any setup or status-checking time.) (10%)

2. Define the following for a cache/main memory structure,
   Cs = Average cost per bit, main memory plus cache
   Cc = Average cost per bit, cache
   Cm = Average cost per bit, main memory
   Sc = Size of cache
   Sm = Size of main memory
   and
   Ts = Average system access time
   Tc = Cache access time
   Tm = Main memory access time
   H = Hit ratio
   (1) Develop a formula for Cs. (7%)
   (2) Develop a formula for Ts. (7%)

3. (1) Describe the organization of FPGA (Field Programmable Gate Array). (7%)
   (2) What are the programmable resources of FPGA (three items) ? (6%)
   (3) What is the programming technology in FPGA. (3%)

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4. Derive an algorithm in flowchart form for the comparison of two signed binary numbers when negative numbers are in signed-2's complement representation:
   (1) By means of a subtraction operation with the signed-2's complement numbers. (13%)
   (2) By scanning and comparing pairs of bits from left to right. (13%)

5. Consider the execution of a program of 15,000 instructions by a linear pipeline processor with a clock rate of 25 MHz. Assume that the instruction pipeline has five stages and that one instruction is issued per clock cycle. The penalties due to branch instructions and out-of-sequence executions are ignored.
   (1) Calculate the speedup factor in using this pipeline to execute the program as compared with the use of an equivalent nonpipelined processor with an equal amount of flow-through delay. (6%)
   (2) What are the efficiency and throughput of this pipelined processor? (6%)

6. Assume that propagation delay along the bus and through the ALU of Figure 1 are 20 and 100 ns, respectively. The time required for a register to copy data from the bus is 10 ns. What is the time that must be allowed for
   (1) transferring data from one register to another? (6%)
   (2) incrementing the program counter? (6%)

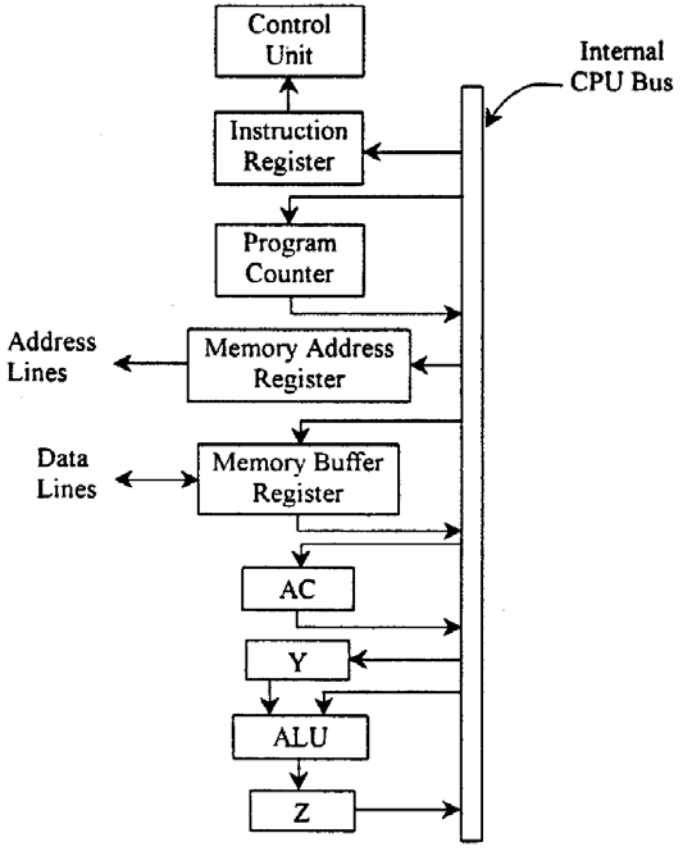

Figure 1