

國立臺灣科技大學
八十八學年度碩士班招生考試試題

系所別：電子工程系碩士班

組別：甲組

科目：計算機組織

I. Brief Questions: Each counts 8%. (40%)

1. Show that how the three factors software, architecture, and hardware technology jointly determine a computer performance.
2. The performance of a 100 MHz microprocessor P is measured by executing 10,000,000 instructions of benchmark code, which is found to take 0.25 s. What are the values of CPI and $MIPS$ for this performance experiment? Is P likely to be superscalar?
3. Estimate the time required to transfer 400 KB from disk to memory given the following disk parameters: seek time, 4ms; rotational delay, 1ms; controller time, $2\mu s$; data transfer rate, 10MB/s.
4. A certain processor has a microinstruction format containing 10 separate control fields $C_0 : C_9$. Each C_i can activate any one of n_i distinct control lines, where n_i is specified as follows:

$i =$	0	1	2	3	4	5	6	7	8	9
$n_i =$	4	4	3	11	9	16	7	1	8	22

What is the minimum number of control bits needed to represent the 10 control fields?
What is the maximum number of control bits needed if a purely horizontal format is used for all the control information?

5. The top of a memory stack contains 3350. The stack pointer SP contains 3240. A two-word procedure call instruction is located in memory at address 2000, followed by the address field of 4385 at location 2001. What are the contents of PC , SP , and the top of the stack:
 - (a) before the call instruction is fetched from memory.
 - (b) after the call instruction is executed.
 - (c) after the return from the procedure.

II. Analysis and Design Problems: Each counts 15%. (60%)

1. A computer can accommodate a maximum of 4G (2^{32}) bytes of main memory. It has a 32-bit word and a 32-bit virtual address and uses 4K byte pages.
 - (a) Assume each page table entry has four bytes. What is the size of page table? Is this size reasonable for a system with tens to hundreds of active programs? If no, give a strategy to solve it.
 - (b) Assuming that the TLB is fully associative and has 32 entries with each containing the Valid, Dirty, and Used bits, the virtual page number, and the physical page number. How many bits of associative memory are required for the TLB? How many bits of SRAM are required for the TLB?

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2. Design a 4-bit magnitude comparator at the register level. Assume that 4-bit binary adder ICs are available as well as ICs containing standard logic gates. The main design goal is to minimize the total number of ICs used.
3. The stack used in Pentium-based computer grows toward the low-address end of M (i.e., memory). Suppose that the stack is required to grow in the opposite direction, that is, toward the high-address end of M.
 - (a) Describe the PUSH and POP instructions needed for this case in RTL (register-transfer level) notations.
 - (b) Design a hardware circuit for implementing the above stack at the register level, assuming that an M -word SRAM IC and register-level components are available. The main design goal is to minimize the total number of ICs used.
4. The hardware cost of a new m -stage, single-function pipeline is approximated by $22m + 25$. The latency of the function to be executed is 85 ns if pipelining is not used. The pipelined implementation's interstage buffers are expected to add an additional $9m\text{ ns}$ to this latency. Estimate the number of stages needed to optimize the pipeline's performance/cost ratio.