國立臺灣科技大學
八十八學年度碩士班招生考試試題

系所別：資訊工程研究所碩士班　　組別：　　科目：計算機概論

1. An unsorted sequence 6,2,1,9,3,8,4,7,5 is stored in an array and to be sorted in increasing order.
   (a) Use heap sort to sort these data (do not insert them one by one). Draw the contents of the array after the first three passes in heap sort, where no extra array is used and the final sorted results are stored in the original array. (9%)
   (b) Write the contents of the first two passes in quick sort, where the first element in the sequence is the pivot and the left sub-sequence is sorted before the right one. (6%)

2. (a) There are three disjoint sets which are represented by trees as shown in Fig.1. Show the parent array which represents the sets. (5%)
   (b) Explain how to apply the two operations "find" and "union" of disjoint set structure in Kruskal's algorithm, which finds a minimum cost spanning tree in a graph. (5%)
   (c) Prove that using weighting rule to merge disjoint set structures can control the height of the tree no greater than $\lfloor \log_2 n \rfloor + 1$. (5%)

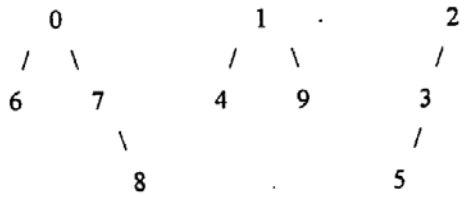

Fig. 1

3. (a) Given a pattern $P = p_1 p_2 \ldots p_m$ and a text $t_1 t_2 \ldots t_n$, please define the *failure function* **f** in Knuth-Morris-Pratt (KMP) pattern matching algorithm. (5%)
   (b) Let $P = p_1 p_2 \ldots p_{10} = abcabcacab$. According to your definition, calculate the corresponding failure function **f** for the given P and save it in the array data structure. (5%)
   (c) Explain why the KMP algorithm has linear-time complexity. (5%)

4. Show that every tree can be transformed into a bipartite graph using linear-time complexity. (5%)

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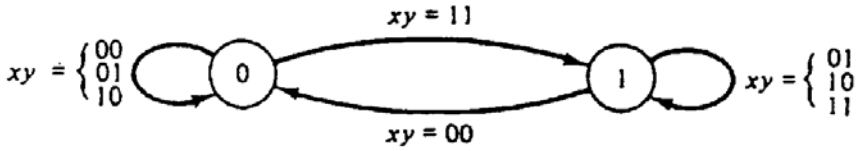
5. Design a sequential circuit for the following state diagram using an RS flip-flop. (10%)



6. Using combinational circuit design techniques, derive the Boolean functions listing in the following table. (10%)

Inputs				Outputs	
I_0	I_1	I_2	I_3	x	y
1	X	X	X	0	0
0	1	X	X	0	1
0	0	1	X	1	0
0	0	0	1	1	1
0	0	0	0	X	X

7. Please draw the block diagram of BCD adder. (10%)

8. An arithmetic circuit has two selection variables S_1 and S_0. The arithmetic operations availabe in the unit are listed below. Determine the circuit that must be incorporated with a full adder in each stage of the arithmetic unit. (10%)

S_1	S_0	$C_1 = 0$	$C_1 = 1$
0	0	$F = A + B$	$F = A + B + 1$
0	1	$F = A$	$F = A + 1$
1	0	$F = \bar{B}$	$F = \bar{B} + 1$
1	1	$F = A + \bar{B}$	$F = A + \bar{B} + 1$

9. Please draw a 4-bit by 3-bit binary multiplier. (10%)