國立臺灣科技大學

八十九學年度碩士班招生考試試題

系所組別： 電子工程系甲組

科　目： 計算機組織

1. Please design a 4-bit up-down binary counter using T Flip-Flops.(18%)

2. Please draw the block diagram of a BCD adder. (15%)

3. Please implement the following Boolean functions with a PLA (15%)

$$F_1 = A\bar{B} + AC + \bar{A}B\bar{C}$$
$$F_2 = AC + BC$$

4. Please design a 4-input priority encoder with inputs and outputs shown in Table 1. (15%)

Table 1. Truth Table of Priority Encoder

Inputs				Outputs		
D_3	D_2	D_1	D_0	A_1	A_0	V
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

5. Table 2 shows the truth table of a full adder.

   (a) Please design the full adder using an eight-input, 2-bit multiplexer. (11%)
   (b) Please design the full adder with a decoder and OR gates (11%)

Table 2. Truth Table of Full Adder

Inputs			Outputs	
x_0	y_0	c_{-1}	s_0	c_0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

6. Fig. 1 shows the procedure gcd to compute the greatest common divisor of two numbers. Fig. 2 shows the hardware needed to implement the gcd procedure. Fig. 3 shows the state table defining the control unit of the gcd processor. Please design the control unit of the gcd processor based on the classical design method using D Flip-Flops and NAND gates. (15%)

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```
gcd(in: X,Y; out: Z);
  register XR, YR, TEMPR;
  XR := X;                      {Input the data}
  YR := Y;
  while XR > 0 do begin
    if XR ≤ YR then begin       {Swap XR and YR}
      TEMPR := YR;
      YR := XR;
      XR := TEMPR; end
      XR := XR – YR;            {Subtract YR from XR}
  end
  Z := YR;                      {Output the result}
end gcd;
```

Fig. 1. Procedure gcd to compute the greatest common divisor of two numbers.

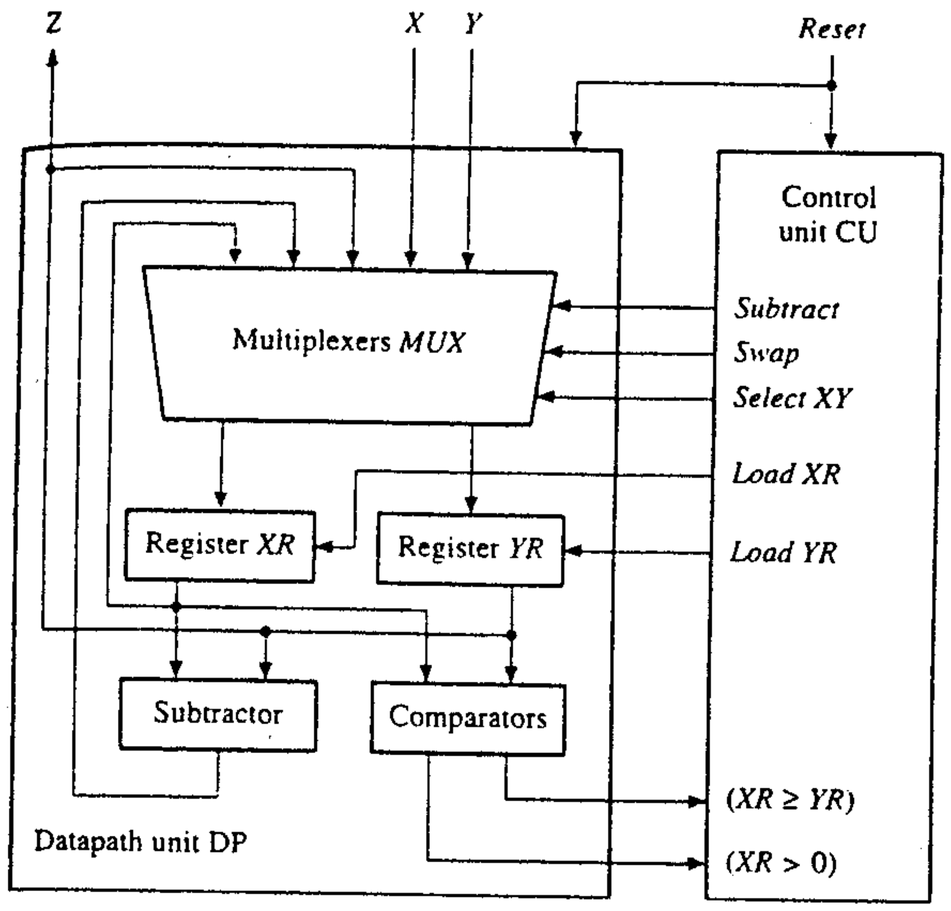

Fig. 2. Hardware needed to implement the gcd procedure.

State	Inputs ($XR > 0$) ($XR \geq YR$) 0–	10	11	Outputs *Subtract*	*Swap*	*Select XY*	*Load XR*	*Load YR*
S_0 (Begin)	S_3	S_1	S_2	0	0	1	1	1
S_1 (Swap)	S_2	S_2	S_2	0	1	0	1	1
S_2 (Subtract)	S_3	S_1	S_2	1	0	0	1	0
S_3 (End)	S_3	S_3	S_3	0	0	0	0	0

Fig. 3. State table defining the control unit of the gcd processor.