國立臺灣科技大學
九十學年度碩士班招生考試試題

系所組別： 電機工程系丙組
科　目： 計算機組織

1. The performance ratio of IBM 360/75 is 50 times that of IBM 360/30, yet the system cycle time is only 5 times as fast. How do you account for this discrepancy? List your reasons and explain. (15%)

2. A DMA module is transferring characters to memory using cycle-stealing, from a device transmitting at 9,600 bps. The CPU is fetching instructions at the rate of 1 million instructions per second (1 MIPS). By how much will the processor be slowed down due to the DMA module. (15%)

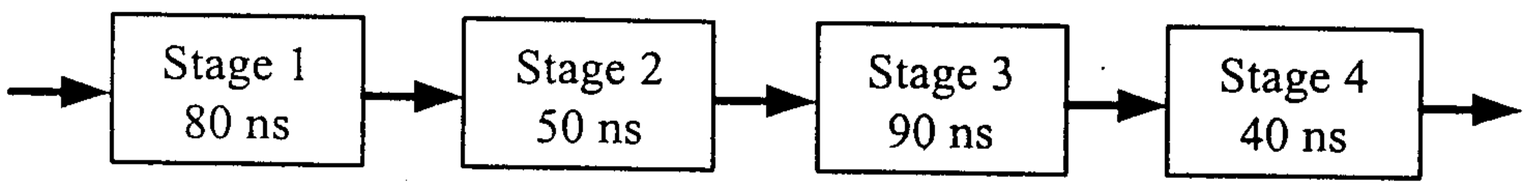
3. The NTUST (National Taiwan University of Science & Technology) computer company has decided to come out with a machine having 16-bit floating numbers. The model 0.001 has a floating point format with a sign bit, 7-bit excess 32 components, and 8-bit mantissa. The model 0.002 has a sign bit, 5-bit excess 32 components, and 10-bit mantissa. Both use radix 2 exponentiation.

   (a) How many decimal digits of precision does each model have? Why? (10%)
   (b) As an electrical engineer, which model would you buy? Why? (10%)

4. A computer system contains a main memory of 32K 16-bit words. It also has a 4K-word cache divided into 4-slot sets with 64 words per slot. Assume that the cache is initially empty. The CPU fetches words from locations 30, 31, 32, ..., 4300 in that order. It then repeats this fetch sequence 5 more times. The cache is 10 times faster than main memory. Estimate the improvement resulting from the use of the cache. Assume an LRU policy for block replacement. (20%)

5. A computer system uses segmentation and paging. The mean segment is s words and the page size is p words. When a segment is in memory, some words are wasted in the last page. In addition, s/p words are "wasted" because they comprise the page table (one word per entry). The smaller the page size, the less waste in the last page of the segment, but the larger the page table. What page size minimizes the total waste? (15%)

6. A *pipeline* machine has four stages, i.e., an instruction consists of four phases (e.g., instruction fetch, instruction decode, operand fetch and execute); Stage 1 needs 80 nanoseconds (ns); Stage 2 needs 50 nanoseconds, and so on. This pipeline is shown as follows: (assuming no other delay) (15%)



   (a) How much time does the pipeline need to complete ten instructions?
   (b) How much time does the pipeline need to complete one hundred instructions?

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21