國立臺灣科技大學
九十二學年度碩士班招生考試試題
系所組別：電子工程系碩士班丙組
科　目：電子學

(1) 20% For a three-input ECL (emitter-coupled logic) OR/NOR gate, as shown in figure 1. Assume a drop of 0.7 V between base and emitter of a conducting transistor. (a) Find the logic levels at the output Y (i.e. find V(0) & V(1)). (b) Calculate R so that the logic levels at Y′are the complements of those at Y.

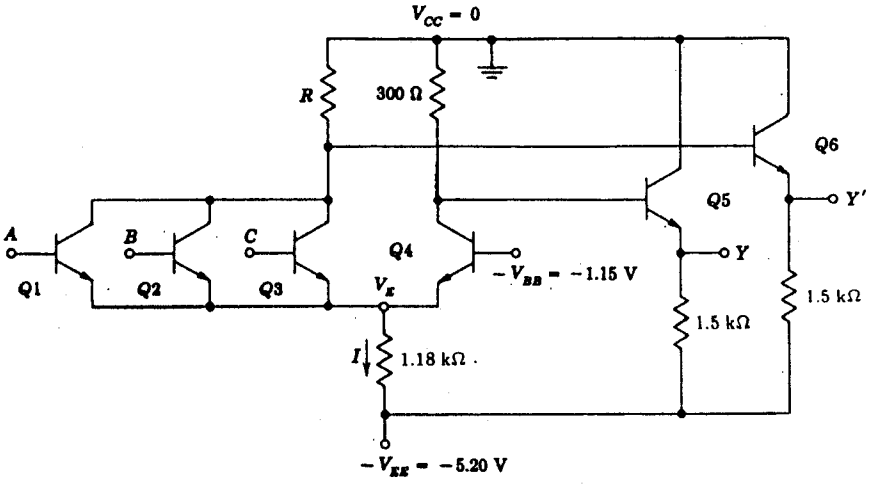

Fig. 1

(2) 15% The small signal low-frequency BJT model is shown in figure 2. For the common-emitter (CE) amplifier shown in figure 3, please find (a) input resistance, (b) voltage gain, (c) voltage gain when hfeRe>>hie.

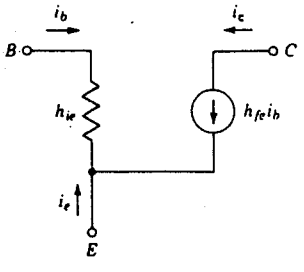

Fig. 2

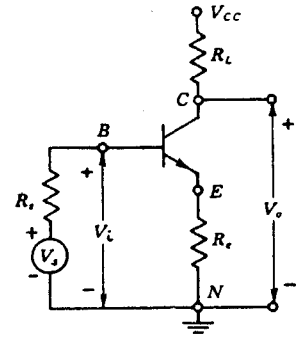

Fig. 3

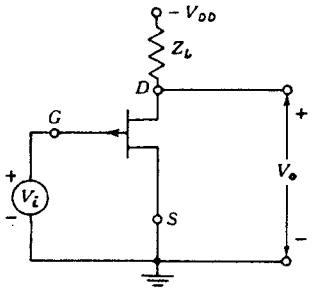

Fig. 4

(3) 15% For the common-source amplifier circuit shown in figure 4, please plot the small signal equivalent circuit at high frequency, and explain the meanings of each item.

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(4) 10% The electron density of a doped silicon crystal is plotted as a function of temperature, shown in figure 5. Please explain the physical meanings of region A, B, and C, respectively.

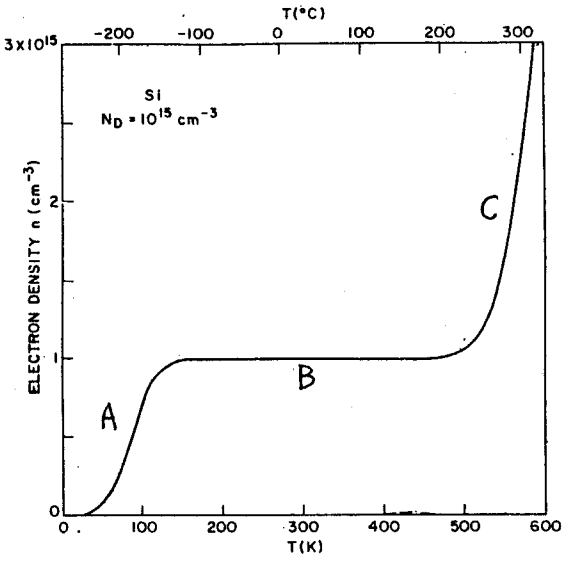

Fig. 5

(5) 10% For a typical BJT, please schematically plot the CE current gain (β) as a function of Ic (i.e. log(β) versus Ic), and explain it.

(6) 10% For a silicon p-n junction, please derive Cj (depletion capacitance per unit area) as a function of ε_s (dielectric constant of silicon) and W (depletion width).

(7) 10% For a typical n-MOSFET, please sketch I_{ds} as a function of V_{ds} for various V_{gs} values with $V_{gs1}>V_{gs2}>V_{gs3}>V_T$, and explain it.

(8) 10% For a typical MOS capacitor with p-type silicon as the substrate, please sketch the capacitance as a function of applied voltage (i.e. C-V profile) at low frequency (10 Hz) and high frequency (100 kHz), respectively, and explain it.