國立臺灣科技大學
九十二學年度碩士班招生考試試題
系所組別：電子工程系碩士班甲組、電機工程系碩士班丙一組
科　目：計算機組織

總分 100 分

(1,2,4,5,6,7) 15 分, (3) 10 分.

1. Why branch prediction is crucial to the performance pipelined CPU? Explain what is 2-bit dynamic branch prediction scheme?
2. Explain why the definition of CPU architecture is based on the ISA (Instruction Set Architecture)? Also compare RISC ISA and CISC ISA, list RISC ISA's advantages and CISC ISA's advantages.
3. What is Translation Lookaside Buffer (TLB)? Explain its purpose.
4. What information should be contained in a DMA controller so that it can do the direct transfer between memory and I/O device?
5. Please compare in detail the cache memory system and virtual memory system.
6. Suppose a CPU has 1024M byte main memory and its cache is 256KB 4-way set-associative with cache line size 32bytes, please describe its cache architecture.
7. Use verilog or VHDL to describe a simple 8-bit ALU. The ALU has the following spec:
   input A, B: 8-bit data, output C: 8-bit data,
   input fun: 2-bit function selection
   C <= A + B when fun = 0,
   C <= A – B when fun = 1,
   C <= A and B when fun = 2,
   C <= A or B when fun = 3.