國立臺灣科技大學
九十三學年度碩士班考試試題

系所組別：電子工程系甲組
科　　目：計算機組織

總分 100 分

1. Suppose we have a computer that uses a memory address word size of 8 bits. This computer has a 16-byte cache and 256 bytes of main memory. The computer accesses a number of memory locations throughout the course of running a program.
Suppose this computer uses direct-mapped cache. The format of a memory address as seen by the cache is shown below:

Tag 4 bits	Block 2 bits	Word 2 bits

The system accesses memory addresses (in hex) in this exact order: 6E, B9, 17, E0, 4E, 4F, 50, 91, A8, A9, AB, AD, 93, and 94. The memory addresses of the first four accesses have been loaded into the cache blocks as shown below. (The contents of the tag are shown in binary in addition to the entire address in hex.)

	Tag Contents	Cache Contents (represented by address)
Block 0	1110	E0
		E1
		E2
		E3

	Tag Contents	Cache Contents (represented by address)
Block 1	0001	14
		15
		16
		17

Block 2	1011	B8
		B9
		BA
		BB

Block 3	0110	6C
		6D
		6E
		6F

(a) What is the hit ratio for the entire memory reference sequence given above? (5%)
(b) What memory blocks will be in the cache after the last address has been accessed? (10%)

2. Please compute the $010101_2 \times 011011_2$ by:
(a) Booth's algorithm looks at 2 bits at a time. (5%)
(b) Booth's algorithm looks at 3 bits at a time. (5%)

3. The most reliable way of determining and reporting performance is execution time of real programs as metric. This execution time is related to these important measurements: clock per instruction (CPI), instruction count (IC) and clock cycle time. Using the following factors, please list their effects on CPI, IC and clock cycle time:
(a) programming skill (3%)
(b) compiler technique (3%)
(c) instruction set design (3%)
(d) computer organization (3%)
(e) semiconductor technology (3%)

4. Please explain three types of pipeline hazards with examples. (15%)

5. Please design a 4-bit carry lookahead adder and a ripple carry adder, and compare the delays for these two adders. (15%)

6. (a) What is branch target buffer (BTB)? If a computer system has BTB, where should it be located (on-chip or off-chip)? Why? Suppose we have a RISC with 5-statge pipeline (instruction fetch (IF), instruction decode (ID), execute (EX), memory access (MEM) and write back (WB)), which of the stage(s) will refer to BTB? Why? (10%)

(b) What is the main purpose of a translation lookaside buffer (TLB)? If a computer system has TLB, where should it be located (on-chip or off-chip)? Why? Suppose we have a RISC with 5-statge pipeline (instruction fetch (IF), instruction decode (ID), execute (EX), memory access (MEM) and write back (WB)), which stage(s) will refer to TLB? Why? (10%)

7. Use verilog or VHDL to design a 4 to 1 multiplex. (10%)
Input data: ina, inb, inc, ind (all 2 bit); intput select control: sel (2bit)
output data: outdata (2bit).
outdata <= ina when sel = 00,
outdata <= inb when sel = 01,
outdata <= inc when sel = 10,
outdata <= ind when sel = 11.