國立臺灣科技大學
九十三學年度碩士班考試試題
系所組別：電子工程系乙一組、電子工程系乙二組、電子工程系乙三組
科　　目：電子電路學

總分 100 分

1. Design an OP-AMP circuit to yield $V_o = 10V_1 + 6V_2 + 4V_3 - 5V_a - 2V_b$. The minimum resistance used should be 10kΩ exactly. Also, try your best to minimize the effect of input bias currents. Assume the OPAMP used in the circuit is ideal except for the input bias currents. (20分)
2. For the circuit shown in Fig-2, analyze the circuit to determine the input resistance, voltage gain, current gain, and output resistance. (30分)

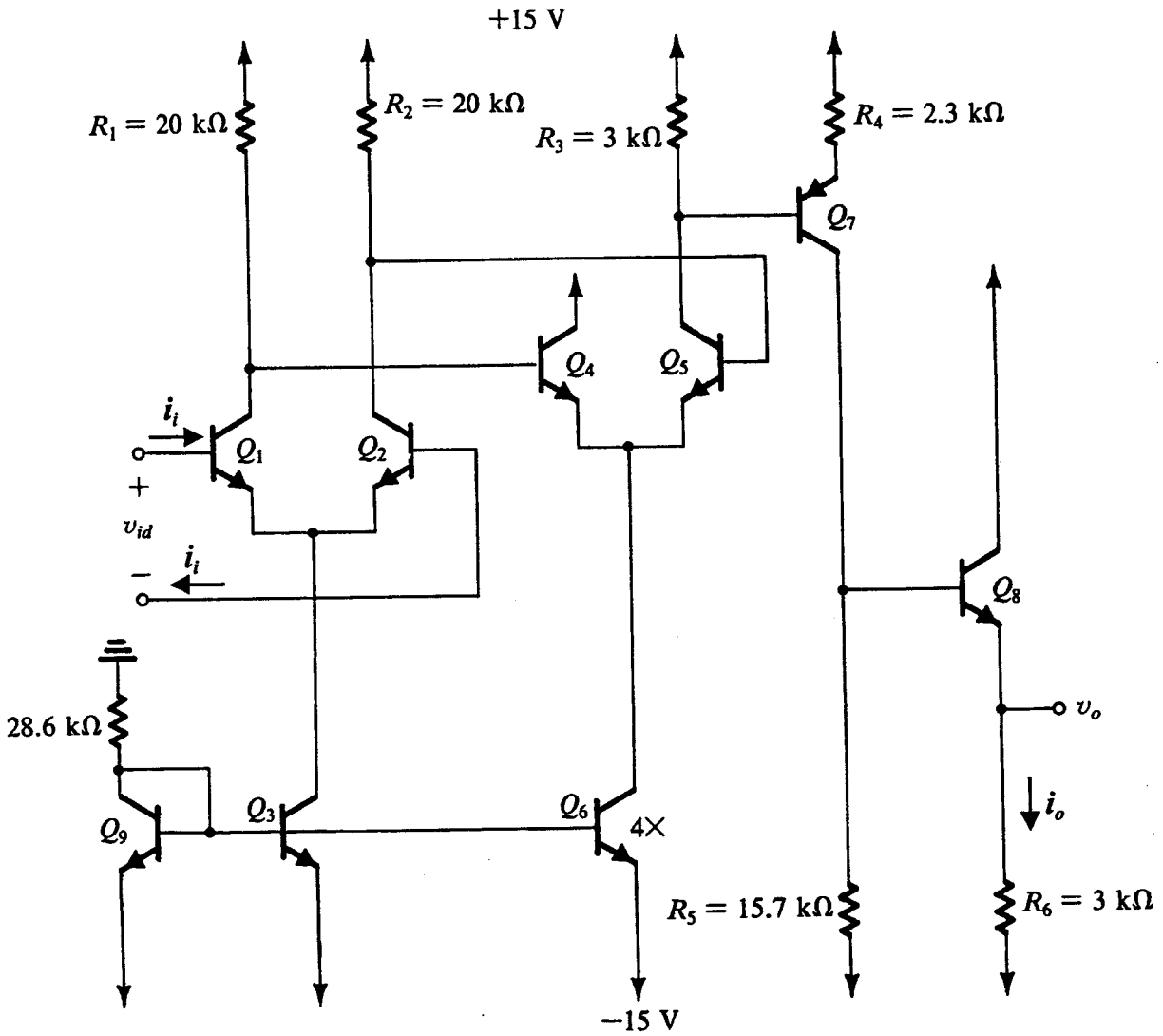

Fig-2

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3. The op amp in the circuit of Fig. 3 has an open-loop gain A(s) with a dc gain of 10^5 and a single pole at 10 rad/s.
   (a) Sketch a Bode plot for the loop gain Aβ(s). (8 分)
   (b) Find the frequency at which |Aβ| = 1. (8 分)
   (c) Find the corresponding gain margin GM. (5 分)
   (d) Specify the closed-loop transfer function. (8 分)

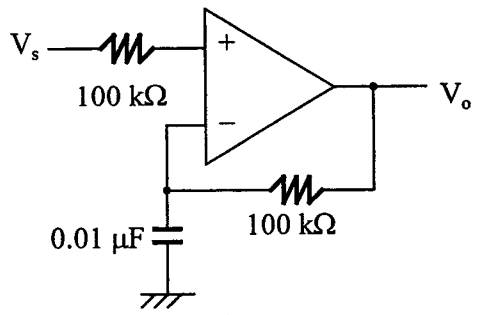

Fig. 3

4. For the limiting circuit shown in Fig. 4, assuming that the op amp is ideal, with V = 10 V, V_D = 0.7 V, R_1 = 50 kΩ, R_2 = R_5 = 10 kΩ, R_3 = R_4 = 5 kΩ:
   (a) Find the limiting levels. (8 分)
   (b) Determine the limiter gain. (5 分)
   (c) Determine the slope in the positive and negative limiting regions. (8 分)

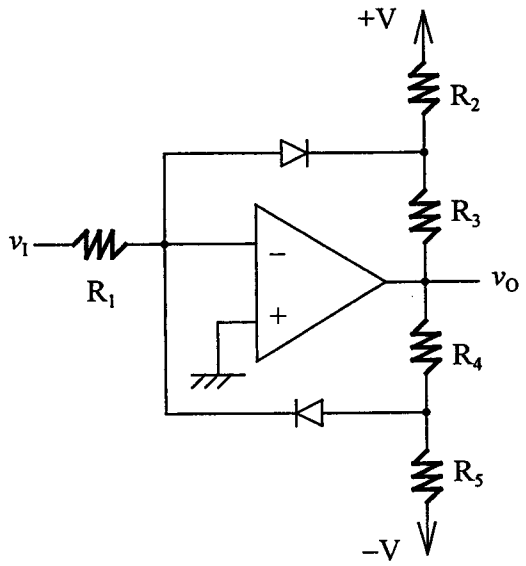

Fig. 4