國立臺灣科技大學
九十三學年度碩士班考試試題

系所組別：電機工程系丙一組
科　　目：計算機組織

總分 100 分

1. (10 points) In some machines, addresses are staggered in two or even more separate main memory units. Explain the purposes of using the technique.

2. (15 points) A computer uses DMA to read from its disk. The disk has 64 512-byte sectors per track. The disk rotation time is 16 msec. The bus is 16 bits wide, and bus transfers take 500 nsec each. The average CPU instruction requires two bus cycles. How much is the CPU slowed down by DMA?

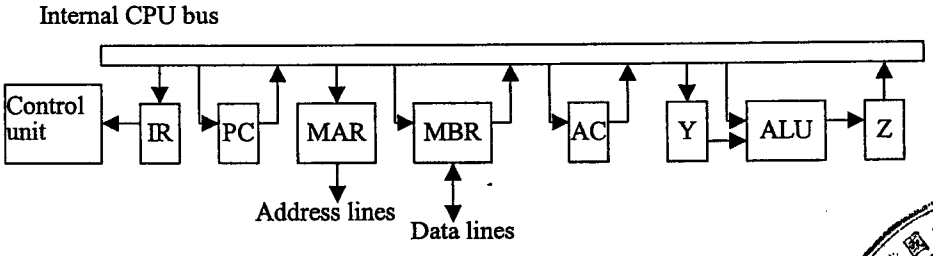
3. (10 points) List of the advantages and disadvantages of memory-mapped I/O compared with isolated I/O.

4. a) (5 points) Suppose we had an n-stage pipeline, what would be the branch penalty be then?
   b) (10 points) Consider a machine on which 30% of the instructions are conditional jumps and another 15% are loop jumps. The loop jumps can be predicted with 60% accuracy and the conditional jumps can be predicted with 90% accuracy. It takes one cycle for no penalty instructions, and the penalty for guessing wrong is four cycles. There is no penalty for unconditional jumps or correct guesses. What is the efficiency of the pipeline on this machine?

5. (10 points) Briefly explain the two basic approaches used to minimize register-memory operations on RISC machines.

6. (10 points) What is the difference between the superscalar and superpipelined approaches?

7. (20 points) Write the sequence of micro-operations required for the bus structure of the following figure to add a number to the AC when the number is
   a. an immediate operand
   b. an indirect-address operand



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8. (10 points) A simple processor has four major phases to its instruction cycle: fetch, indirect, execute, and interrupt. Two 1-bit flags designate the current phase in a hardwired implementation.
   a. Why are these flags needed?
   b. Why are they not needed in a microprogrammed control unit?