國立臺灣科技大學
九十四學年度碩士班招生考試試題

系所組別：電子工程系碩士班甲組
科　　目：計算機組織

總分100分，所有答案必須寫在答案卷上.

計算機組織 Computer Organization

1. (21%) In a memory hierarchy with a TLB and a cache, a memory reference can have three different types of misses: a TLB miss, a page fault, and a cache miss. Please consider the combinations of these three events to state whether this event can actually occur and under what situations。

TLB	Page table	Cache	Possible? If so, under what situations
Hit	Hit	Miss	
Miss	Hit	Hit	
Miss	Hit	Miss	
Miss	Miss	Miss	
Hit	Miss	Miss	
Hit	Miss	Hit	
Miss	Miss	Hit	

2. (10%) Please explain the following terms.
   (a) Moore's Law (2%)
   (b) Rock's Law. (2%)
   (b) Tournament branch predictor? (3%)
   (d) Trace cache (3%)

3. (10%) The first two bytes of a 2Mx16 main memory have the following hex values:
   Byte 0 is FE
   Byte 1 is 01
   If these bytes hold a 16-bit 2's complement integer, what is its actual decimal values if:
   (a) memory is big endian (5%)
   (b) memory is little endian (5%)

4. (9 %) Please answer the following problems in detail.
   (a) What is the difference between VLIW and superscalar? Which model, VLIW or superscalar, presents the greater challenge for compilers? Why? (5%)
   (b) What is the shortcoming of using MIPS or FLOPS as a measure of system throughput? (4%)

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5. The switching algebra (i.e., two-valued Boolean algebra) is defined on the following three operators: OR, AND, NOT. Thus, any logic module that can realize these three operators can be used to implement any switching functions (two-valued Boolean functions) without requiring any other logic elements.

(a) (12%) Show that any switching function can be realized only by using 4-to-1 multiplexers.

(b) (4%) Design a 3-to-1 multiplexer using only two 2-to-1 multiplexers.

(c) (4%) Design a 4-to-1 multiplexer using only three 2-to-1 multiplexers.

6. Cache memory is commonly used in modern microprocessors. Assume that a two-way set-associative cache memory is used in some modern microprocessor. Each block within the appropriate set of the cache memory contains three fields: a V bit to indicate whether the entry is valid or not, an n-bit tag, and 8-bit data. The address and data buses of the microprocessor are 16 bits and 8 bits, respectively.

(a) (4%) How many bits are required for the tag field in each cache block of the cache memory if each set of the cache memory has 64 cache blocks?

(b) (6%) Assume that the input of the cache memory module is a 16-bit address and the output contains one hit bit to indicate hit or not and the required data output if hit. Draw the block diagram of the cache memory module.

7. Assume that you have a lot of basic two-input gates: AND, OR, XOR, XNOR, and NAND, and enough 32×4 high-speed SRAMs (static RAMs). The basic gates have propagation delay 0.4 ns and SRAM has access time 1.2 ns, ignoring all wire delays. You are asked to design a two-way set-associative cache memory module satisfying the following conditions:

(1). Each set of the cache memory has 64 cache blocks and each cache block contains three fields: a V bit to indicate whether the entry is valid or not, an n-bit tag, and 8-bit data.

(2). The input of the cache memory module is a 16-bit address and the output contains one **hit** bit to indicate hit or not and the required data output if hit.

(3). Assume that all tag values are different at any time.

(a) (6%) How many SRAMs are required for the cache memory module?

(b) (14%) Can we design this cache memory module using the given basic gates and SRAM modules if the access time of the cache memory module must limit within 5 ns? If your answer is yes, show how to do it; if your answer is no, give your reasons.

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