國立臺灣科技大學

九十四學年度碩士班招生考試試題

系所組別：電子工程系碩士班乙一組、乙二組、乙三組

科　　目：電子學

總分100分

1. Consider the complementary BJT class B output stage as shown in Fig. P1 and neglect the effects of V_{BE} and V_{CEsat}. For ±10-V power supplies and a 100-Ω load resistance, **(1)** what is the maximum sine-wave output power available $P_{L,max}$=? **(2)** What is the power conversion efficiency η_1=? For output signals of half this amplitude ($V_{o,max}$/2), **(3)** find the output power P_L=?, **(4)** the supply power P_{CC}=?, and **(5)** the power conversion efficiency η_2=? (20%)

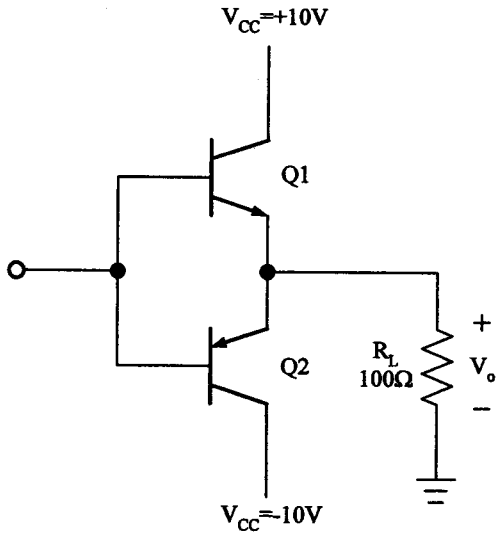

Fig. 1

2. For the circuit shown in Fig. P2, **(1)** find g_{m1}, g_{m2}, and the mid-band gain A_M=? and **(2)** the upper 3-dB frequency f_H= f_{-3dB}=?. For the BJT, β= 200, C_μ= 0.8pF, and f_T= 600MHz. For the NMOS, V_t= 1V, $k'W/L$= 2mA/V^2, and C_{gs}=C_{gd}= 1pF. **(3)** Find C=? for a low cutoff of 10Hz. (20%)

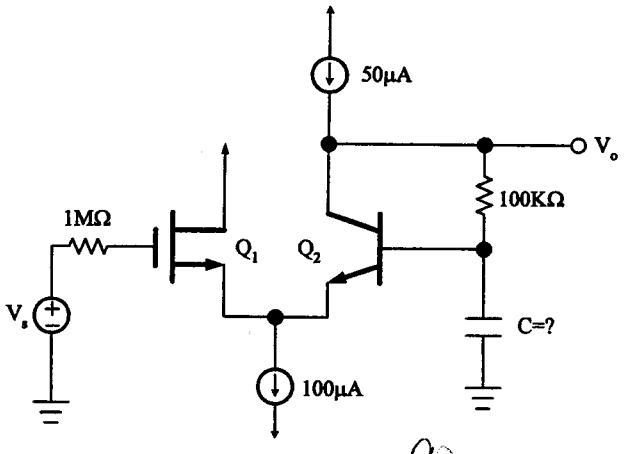

Fig. P2

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3. For the two-terminal circuit of Fig. P3, known as the V_{BE}-multiplier, assume I to be a sufficiently large and β to be very high and find expressions for (1) the dc voltage drop V_x=? and (2) the incremental reisstance r_x=? between X and ground. (3) find the values of V_x=? and r_x=? for R_1=R_2=1 kΩ, I=10mA, and V_{BE}=0.7V. (10%)

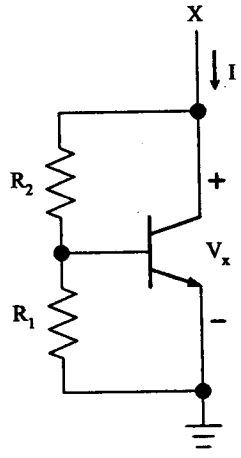

Fig. P3

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4. (15%) For the circuit shown in Fig. 1, deduce the voltage gain v_o / v_{id}. Assume ideal OPAMP is used.

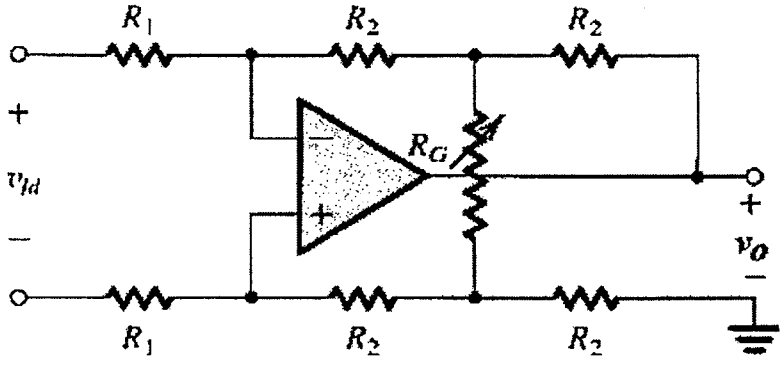

Fig. 1

5. (20%) Refer to the circuit in Fig. 2 where the output resistance of current source I is R_{SS}:,

(a) Let the two drain resistors be denoted R_{D1} and R_{D2} where $R_{D1} = R_D + \Delta R_D / 2$ and $R_{D2} = R_D - \Delta R_D / 2$ ($\Delta R_D \ll R_D$). Also let $g_{m1} = g_m + \Delta g_m / 2$ and $g_{m2} = g_m - \Delta g_m / 2$ ($\Delta g_m \ll g_m$) where g_{m1} and g_{m2} are the transconductances of Q_1 and Q_2 respectively. Please find the CMRR of the circuit in Fig. 2.

(b) If the bias current I is increased with R_{SS}, $\Delta g_m / g_m$, $\Delta R_D / R_D$ and other circuit parameters unchanged, will the CMRR be increased, decreased, or kept the same? Deduce or explain your answer.

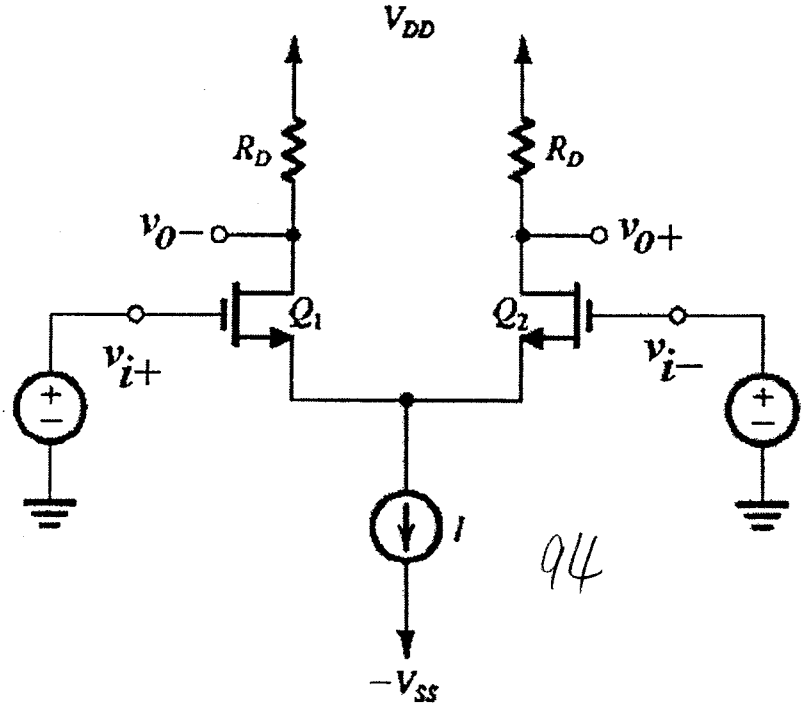

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Fig. 2

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6. (15%) The amplifier in the feedback system shown Fig. 3(a) has an open loop gain A with amplitude and phase shown in Fig. 3(b):

(a) Is the open-loop amplifier with gain A stable? How many poles and zeroes does it have?

(b) If the feedback system is required to have a 45° phase margin for its closed-loop gain, then β=? Assume β is frequency-independent.

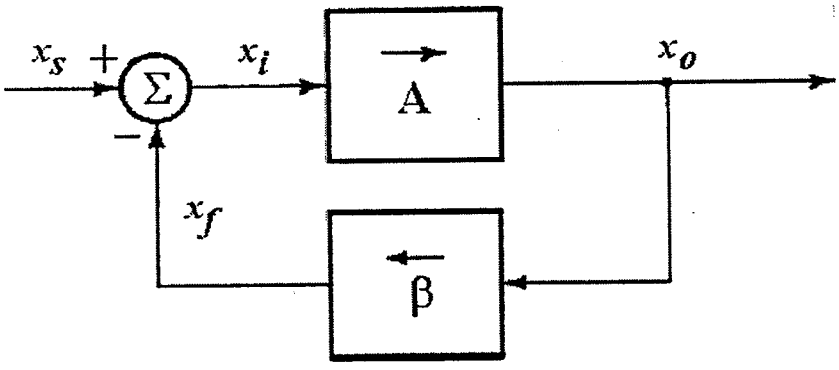

Fig. 3(a)

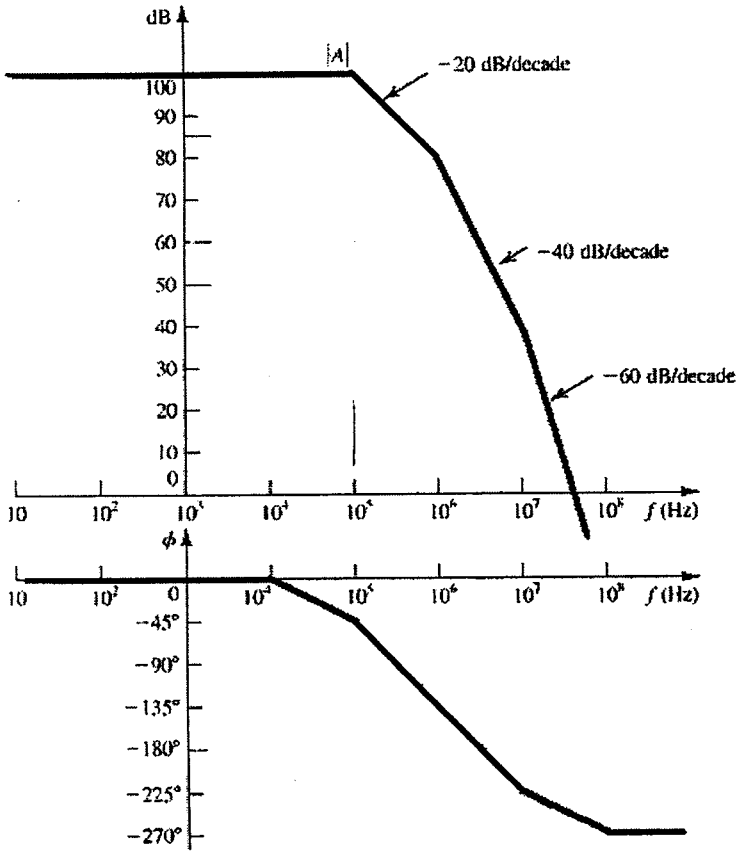

Fig. 3(b)

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