國立臺灣科技大學

九十四學年度碩士班招生考試試題

系所組別：電機工程系碩士班乙二組、電機工程系碩士班丙二組

科　　目：電子學

總分100分

1. Consider a peak rectifier fed by a 60-Hz sinusoid having a peak value V_p=160V, as shown in Figure 1. Let the load resistance R = 16kΩ.

(a) Find the value of the capacitance C that will result in a peak-to-peak ripple of 5V. (10%)

(b) Draw approximately the voltage waveforms v_I and v_o in the peak rectifier circuit. (10%)

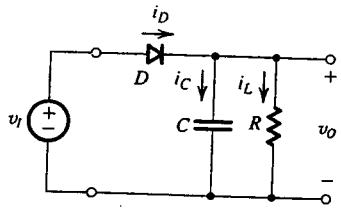

Figure 1

2. (a) Design the circuit shown in Figure 2 so that the transistor operates in saturation with I_D = 0.5 mA and V_D=+3V. Let the enhancement-type PMOS transistor have V_t = −1 V and $k'_p(W/L) = 1\ \text{mA/V}^2$. Neglect the channel-length modulation effect. (15%)

(b) What is the largest value that R_D can have while maintaining saturation-region operation? (5%)

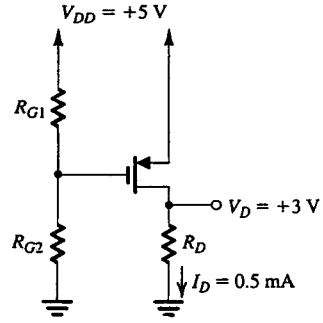

Figure 2

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Problem 3:
For the following circuit that uses shunt-series feedback.

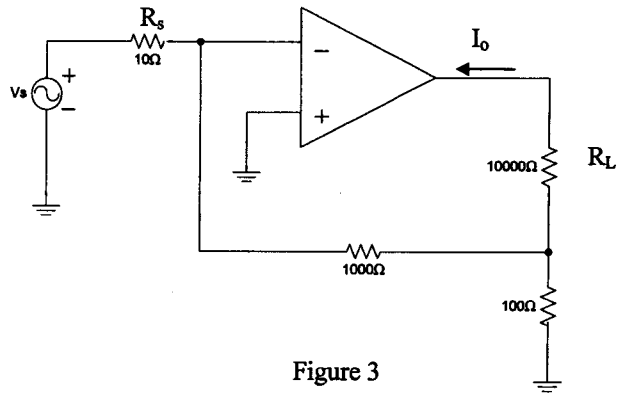

Figure 3

(a) Find the closed loop gain I_o / I_s. (10%)
(b) The input resistance R_{in} (not including R_s). (5%)
(c) The output resistance R_{out} (not including R_L). (5%)

For the op-amp plotted in Figure 3, some available parameters are listed below:
1. Open loop voltage gain of 10,000 V
2. Differential input resistance = 100,000 Ω
3. Output resistance = 1000 Ω

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Problem 4:

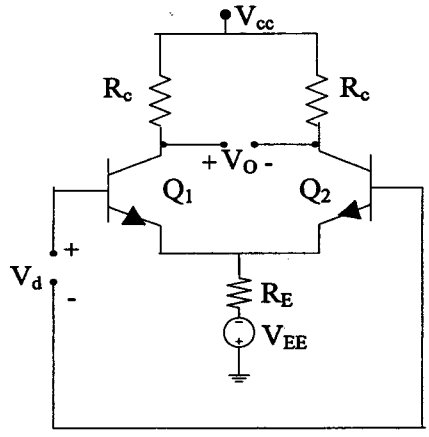

Figure 4

Some available parameters are listed below:

1. $Q_1 = Q_2$
2. $V_{cc} = 15$ V
3. $V_T = 0.026$ V
4. $V_A = 80$ V
5. $\beta = 400$
6. $R_C = 20k\,\Omega$
7. $R_E = 28.6k\,\Omega$

($1k = 1000$)

Using half circuit models to find out

(a) The differential gain A_d (5%)

(b) The common-node gain A_{cm} (5%)

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5. We wish to analyze the transistor amplifier shown in Figure 5 to determine its voltage gain for small signal operation. Please answer the following questions:
(a) Determine the small signal parameters of r_e, g_m and r_π. (10%)
(b) Determine the voltage gain $A_v = v_o/v_i$. (10%)

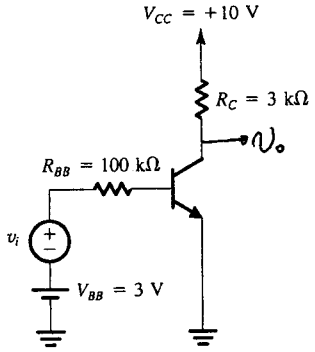

Figure 5

6. Figure 6 shows an ideal voltage amplifier having a gain of -100V/V with an impedance Z of 1-pF capacitance connected between its output and input terminals.
(a) Draw the equivalent Miller equivalent circuit. (5%)
(b) Derive the transfer function of $V_o(s)/V_{sig}(s)$. (5%)

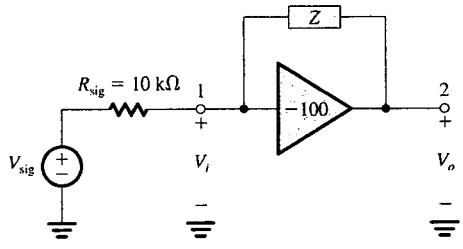

Figure 6