國立臺灣科技大學
九十四學年度碩士班招生考試試題

系所組別：電機工程系碩士班丙一組
科　　目：計算機組織

總分100分

1. A 5-way set-associative cache consists of a total of 160 blocks, with 5 blocks in each set. Each block has 32 words. The main memory contains 8192 blocks. Assume the machine is word-addressable.
   a. How many bits are there in a main memory address? (4%)
   b. How many bits are there in each of the TAG, SET, and OFFSET fields? (6%)

2. The SEAS 16-bit floating point standard is just like the "IEEE floating point standard" except that it uses 1 bit for the sign, 5 bits for the exponent, and 10 bits for the fraction (or mantissa, normalized). The exponent is in excess 15 representation.
   a. What is the decimal representation of the following SEAS floating point number?
   0 01001 0101000000 (6%)
   b. What is the "SEAS standard 16-bit" representation of the decimal number -50.75 ? (6%)

3. Pipeline Processor Design:
   a. How will pipeline hazard happen? (4%)
   b. Design a pipeline adder that can add six separate bit streams. (i.e., binary numbers) (12%)

4. A 600MHz CPU (code name *Mbase*) has the following characteristics: (12%)

Instruction Set	CPI	Frequency
A	2	50%
B	3	10%
C	2	20%
D	5	20%

   a. The following improvements are made to *Mbase* to produce a new machine (*Mfast*):
      i. The clock rate is increased to 650MHz
      ii. The hardware is improved so that Class D instructions take 4 cycles
      iii. The compiler is improved so that 5% fewer Class A and Class C instructions are generated for the same code compared to the base machine
      Based on the above data, how much faster is the new machine *Mfast* compared to *Mbase*? Express your answer as a percentage.
   b. Suppose the *Mfast* is K times faster than *MBase*. If Program A is run on both machines and 30% of program A execution time is I/O access. The I/O access is 10% faster on *Mfast* than on *Mbase*. How much faster will Program A run on *Mfast* than on *Mbase*?

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5. Please design a computer system with 8-bit data bus, and 1MB memory. You are required to use 2^{17}-byte SRAMs chips having a chip select ($\overline{CS}$) input and a control signal ($R/\overline{W}$), and a 3-to-8 line decoder as your decoder. (15%)

6. Design a circuit to convert an incoming parallel 32-bit word from big-ending form to little-ending form. (10%)

7. Design the hardware to signal a parity error if the 8-bit value in the register is not odd parity. (10%)

8. Numerical value A and B are stored in computer as approximations A' and B'. Neglecting any further truncation or roundoff errors, show that the relative error of the product is approximately the sum of the relative errors in the factors. (15%)

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