國立台灣科技大學九十五學年度碩士班招生試題

系所組別： 電子工程系碩士班甲組

科　　目： 計算機組織

Total: 100 points

1. Assume that a certain task needs p CISC instructions and $2p$ RISC instructions, and that one CISC instruction takes $8T$ ns to complete, and one RISC instruction take $2T$ ns. Please evaluate which one has the better performance. (5%)
2. Consider two different implementations M_1 and M_2 of the same instruction set. M_1 has a clock frequency of 500MHz. M_2's clock cycle is 1.5 ns. There are three classes of instructions with the following CPIs:

Class	CPI for M_1	CPI for M_2
A	2	2
B	1	2
C	3	4

   a What are the peak performances of M_1 and M_2 expressed at MIPS? (5%)

   b If the number of instructions executed in a certain program is divided equally among the three classes, which machine is faster and by what factor? (10%)

   c We can redesign M_2 such that with negligible cost increase, the CPI for class-B instructions improves from 2 to 1 (class-A and class-C CPIs remain unchanged). This change, however, would increase the clock cycle from 1.5 ns to 2 ns. What should the minimum percentage of class-B instructions be in an instruction mix of this redesign to result in improved performance? (10%)

3. A computer system uses two levels of cache L1 and L2. Level L1 is accessed in one clock cycle and supplies the data in case of an L1 hit. For an L1 miss, occurring 3% of the time, L2 is consulted. An L2 hit incurs a penalty of 10 clock cycles while an L2 miss implies a 100-cycle penalty.

   a Assuming pipelined implementation with a CPI of 1 when there is no cache-miss whatsoever (i.e., ignoring data and control dependencies), calculate the effect CPI if L2's local miss rate is 25%. (5%)

   b If we were to model the two-level cache system as a single cache, what miss rate and miss penalty should we use? (5%)

   c Changing the mapping scheme of L2 from direct to two-way set-associative can improve its local miss rate to 22% while increasing its hit penalty to 11 clock cycles owing to the more complex access scheme. Ignoring cost issues, is this change a good idea? (10%)

國立台灣科技大學九十五學年度碩士班招生試題

系所組別： 電子工程系碩士班甲組

科　　目： 計算機組織

4. A certain memory system has a 32 MB main memory, and a 64 kB cache, where $k = 1,024$. Blocks are 16 bytes in size. Show the fields in a memory address if the cache is:

   1. associative (5%)
   2. direct-mapped (5%)
   3. 8-way set-associative. (5%)

5. Suppose that we want to design a three-port register file. The register file consists of four registers, each of which is 4 bits. There are two read ports and one write port. To access a read or write port, we need to apply a register address, and an access control signal: read or write. Using components from the set {AND, OR, NOT, decoder, encoder, multiplexer, demultiplexer, D-type flip-flops}, answer the following questions.

   1. (4%) Design a 4-bit register with paralle-load control using D-type flip-flops. Please note that you have to guarantee the register work properly at minimum cost in terms of number of gates.
   2. (16%) Using components from the set {AND, OR, NOT, decoder, encoder, multiplexer, demultiplexer, D-type flip-flops}, design this register file.

6. Memory hierarchy (or called multilevel memory system) is commonly used in modern computer systems. Answer the following questions about the memory hierarchy.

   1. (6%) Draw a block diagram showing the memory hierarchy in the typical computer systems and show the cache memory subhierarchy and virtual memory subhierarchy.
   2. (3%) Explain the principle behind the memory hierarchy (i.e., explain why the memory hierarchy is used, what its purpose is, and why it can accomplish the required objects.)
   3. (6%) List the major differences between cache-main and main-secondary-memory hierarchies in terms of typical access time ratio, memory management system (i.e., implemented by software or hardware or both), typical block size, and access method of processor to second level (i.e., direct access or indirect access).

85.