國立台灣科技大學九十六學年度碩士班招生試題

系所組別： 電子工程系碩士班甲組

科　　目： 計算機組織

總分100分

1. Given the number 0x811F00FE, what is it interpreted as:
   (a) Four two's complement bytes? (3%)
   (b) Four unsigned bytes? (3%)

2. Given the following instruction mix, what is the CPI for this processor? (4%)

Operation	Frequency	CPI
A	50%	1
B	15%	4
C	15%	3
D	10%	4
E	5%	1
F	5%	2

3. The following piece of code has pipeline hazard(s) in it. Please try to reorder the instructions and insert the **minimum** number of NOP to make it hazard-free. (Note: Assume all the necessary forwarding logics exist) (10%)

```
haz:    move    $5, $0
        lw      $10, 1000($20)
        addiu   $20, $20, -4
        addu    $5, $5, $10
        bne     $20, $0, haz
```

4. Given a MIPS machine with 2-way set-associative cache that has 2-word blocks and a total size of 32 words. Assume that the cache is initially empty, and that it uses an LRU replacement policy. Given the following memory accesses in sequence:

```
0ff00f70
0ff00f60
0fe0012c
0ff00f5c
0fe0012c
0fe001e8
0f000f64
0f000144
0fe00204
0ff00f74
0f000f64
0f000128
```

   (a) Please label whether they will be hits or misses. (6%)
   (b) Please calculate the hit rate. (4%)

5. The speed of the memory system affects the designer's decision on the size of the cache block. Which of the following cache designer guidelines are generally valid? why? (10%)

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(a) The shorter the memory latency, the smaller the cache block.
(b) The shorter the memory latency, the larger the block.
(c) The higher the memory bandwidth, the smaller the cache block.
(d) The higher the memory bandwidth, the larger the cache block.

6. Please state whether the following techniques are associated primarily with a software- or hardware-based approach to exploiting ILP. In some cases, the answer may be both. (10%)
   (a) Brach prediction
   (b) Dynamic scheduling
   (c) Our-of-order execution
   (d) EPIC
   (e) Speculation
   (f) Multiple issue
   (g) Superscalar
   (h) Reorder buffer
   (i) Register renaming
   (j) Predication

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7. What is Saturating Arithmetic? What kind of instructions use this feature? (8%)
8. Please describe the Shift-and-Add multiplier architecture and its control steps. (12%)
9. What fields are contained in TLB (translation lookaside buffer)? What are the purposes of these fields? (8%)
10. How many tag-comparators are needed in a 2-way set associative cache controller? Why?(4%)
11. What is Cache Line Width? Why is it larger than the word-size of CPU? (6%)
12. Use Verilog or VHDL languages to design a one-bit 8-to-1 multiplexer circuit. (12%)