國立台灣科技大學九十七學年度碩士班招生試題

系所組別： 電子工程系碩士班甲組

科　　目： 計算機組織

總分 100分

1. (5%) Assume that a CPU can perform a multiplication operation in 10ns, and a subtraction operation in 1ns. How long will it take for the CPU to calculate the result of $d = a \times b - a \times c$? Could you optimize the equation so that it will take less time?

2. (10%) Please explain the following terms:
   - Dynamic power (2%)
   - Translation-lookaside buffer (TLB) (2%)
   - Reorder Buffer (2%)
   - Data hazard (2%)
   - Brach target buffer (BTB) (2%)

3. (10%) Consider three branch prediction schemes: branch not taken, predict taken, and dynamic prediction. Assume that they all have zero penalty when they predict correctly and 2 cycles when they are wrong. Assume that the average predict accuracy of the dynamic predictor is 90%. Please explain which predictor is the best choice for the following branches?
   - A branch that is taken with 5% frequency (3%)
   - A branch that is taken with 95% frequency (3%)
   - A branch that is taken with 70% frequency (4%)

4. (10%) As the following statements are completely accurate?
   - The Pentium 4 can issue more instructions per clock than the Pentium III. (2%)
   - In reducing misses, associativity is more important than capacity. (2%)
   - The Pentium 4 uses dynamic scheduling with speculation. (2%)
   - The clock rate for the dual-core is higher than the Pentium 4. (2%)
   - The basic microarchitecture of the Pentium III and the Pentium 4 is similar. (2%)

5. (10%) Consider three processors with different cache configurations:
   - Cache 1: Direct-mapped with one-word blocks
   - Cache 2: Direct-mapped with four-word blocks
   - Cache 3: Two-way set associative with four-word blocks

   The following miss rate measurements have been made:
   - Cache 1: Instruction miss rate is 4%; data miss rate is 6%
   - Cache 2: Instruction miss rate is 2%; data miss rate is 4%

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- Cache 3: Instruction miss rate is 2%; data miss rate is 3%

For these processors, one-half of the instructions contain a data reference. Assume that the cache miss penalty is 6+Block size in words. The CPI for this workload was measured on a processor with cache 1 and was found to be 2.0. Determine which processor spends the most cycles on cache misses.

6. (5%) Does a TLB miss imply a page fault? Explain your answer.
7. (4%) The register r0 in MIPS CPU is hardwired to zero, what is its purpose? Please provide an example for its purpose.
8. (10%) The instruction encoding of RISCs uses fixed length instruction, please discuss its advantages and disadvantages.
9. (6%) Can a pipelined single-instruction issue CPU achieve the performance with CPI less than or equal 1. Why?
10. (6%) What is the IPC performance limit for a dual-issue superscalar? Why?
11. (8%) If you write the following C code in a big-endian CPU, what will be the output in the console?

```
char *cp;
long data = 0x12345678;
cp = (char *) &data;
printf( "%x", *(cp+2) );
```

12. (6%) Design a circuit which can convert 8-bit singed integer to 16-bit signed integer. The input is A7, A6, …, A0 (A7 is MSB). The output is B15, B14, …, B0, (B15 is The MSB).
13. (10%) Use Verilog or VHDL to design a 4-bit 3 to 1 multiplexer.

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