國立台灣科技大學九十七學年度碩士班招生試題

系所組別： 電機工程系碩士班丁組

科　　目： 邏輯設計

本試題總分: 100

Problem #1 (18%)

(a) Give the 6-bit sign-magnitude, 1's complement, and 2's complement representations for decimal 3 and –7.

(b) Convert decimal 51768 into hexadecimal, octal, and binary.

Problem #2 (12%)

(a) Given f(a, b, c, d)=Σm(0, 2, 5, 7, 8, 10, 13, 15). Find the minimum POS and SOP expressions by using a Karnaugh map.

(b) Given f(a, b, c, d, e)=Σm(0, 1, 6, 10, 12, 14, 16, 17, 26, 30) . Find the minimum SOP expression using a 5-variable K-map.

Problem #3 (10%)

(a) Use NOR gates to draw the circuit for the function F = abc'+ab'c'+a'bc

(b) Use NAND gates to implement $f_{abc} = \prod M(0, 3, 5, 7)$.

Problem #4 (10%)

Realize f(a, b, c)=Σm(2, 4, 5, 7) with a 4-to-1 multiplexer module.

Problem #5 (10%)

A PN flip-flop has four operations, clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively.

(a) Show the characteristic table.

(b) Show the characteristic equation.

Problem #6 (10%)

A sequential circuit has two JK flip-flops A and B and one input x. The circuit is described by the following flip-flop input equations:

$J_A=B, K_A=Bx'$

$J_B=x', K_B=A'x+Ax'$

(a) Derive the state equations A(t+1) and B(t+1) by substituting the input equations for the J and K variables.

(b) Draw the state diagram of the circuit.

Problem #7 (10%)

Draw the logic diagram of a four-bit register with four D flip-flops and four 4*1 multiplexers with mode selection inputs S_1 and S_0. The register operates according to the following function table:

S_1	S_0	Register Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

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Problem #8 (20%)

It is necessary to formulate the Hamming code for four data bits, D_3, D_5, D_6 and D_7, together with three parity bits, P_1, P_2 and P_4.

(a) Evaluate the 7-bit composite code word for the data word 0010.

(b) Evaluate three check bits, C4, C2 and C1, assuming no error.

(c) Assume an error in bit D5 during writing into memory. Show how the error in the bit is detected and corrected.

(d) Add parity bit P8 to include double-error detection in the code. Assume that error occurred in bit P2 and D5. Show how the double error is detected.