國立台灣科技大學九十八學年度碩士班招生試題

系所組別： 電機工程系碩士班丁組

科　　目： 邏輯設計

（總分爲 100 分）

# Logic design

**Problem #1 (20%)**

Perform each of the following arithmetic operations of 8-bit 2's complement signed numbers:

(a) 11100111 + 00010011

(b) 11100111 - 00010011

(c) 01010011 * 00000111 (write down your result in 16-bit)

(d) 01010011 * 11000101 (write down your result in 16-bit)

**Problem #2 (10%)**

(a) Convert the standard SOP expression $f = \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}C + ABC$, to an equivalent standard POS expression.

(b) Using a Karnaugh map, convert the minimum POS expression $f(A,B,C,D) = (A + B + \overline{C})(\overline{B} + C + D)(B + C + \overline{D})$, into a minimum SOP expression.

**Problem #3 (10%)**

Use an 8-line multiplexer to implement the function f(A,B,C,D)=Σm(0,1,5,6,7,11,13), in which signals A,B,C are the 3 address lines, and signal D is used as the data input signal.

**Problem #4 (10%)**

Please use inverters, AND gates, and XOR gates to constitute a 3-input OR gate.

**Problem #5 (10%)**

Determine the period (in terms of the clock cycles) of an *n*-bit Johnson counter.

**Problem #6 (20%)**

Complete your design in logic circuit, Verilog code, or VHDL code to realize the following state diagram.

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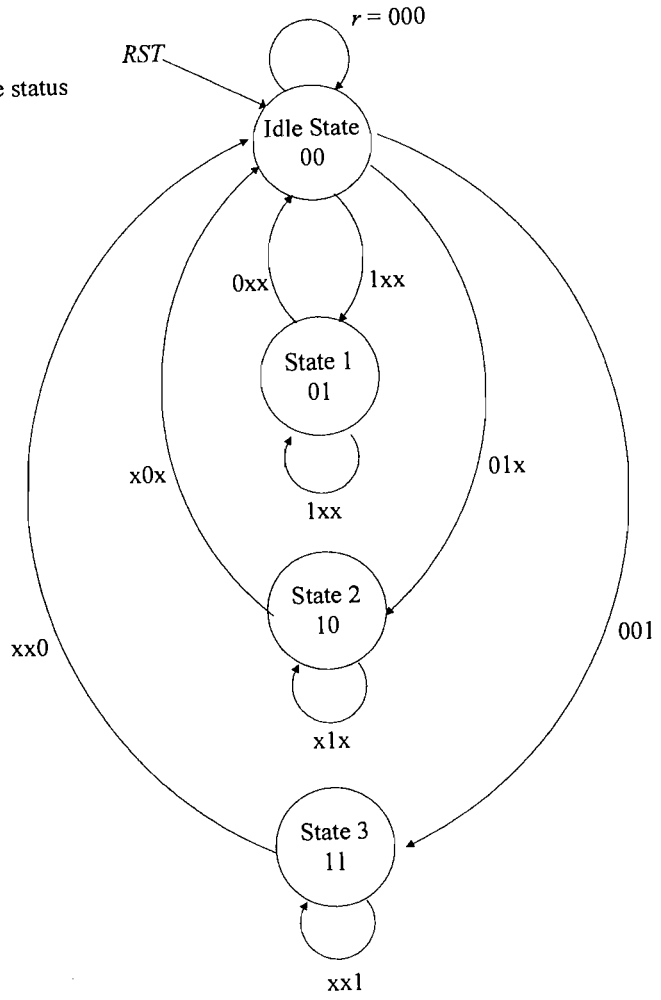
Input signal: $r$
Reset signal: $RST$
Output signal: $y$ = state status




**Problem #7 (20%)**

Design a circuit that can generate a short pulse that extends to two clock period for the following timing diagram.