

國立台灣科技大學九十九學年度碩士班招生試題

系所組別：電子工程系碩士班甲組

科目：計算機系統

(總分為100分)

[計算機組織]

- (8%) Please describe the difference between CISC and RISC machines, and give an example for each of them.
- (12%) In the pipeline structure, there are situations called hazards that the next instruction cannot execute in the following clock cycle. Based on the different causes, hazards can be divided into three types: structural, data and control hazards. Please explain the cause of each type in detail.
- (6%) Suppose we have a 32-bit computer with an instruction set that supports immediate instructions as shown below:

| Operand | Source Register | Destination Register | Immediate |
|---------|-----------------|----------------------|-----------|
| 6 bits | 5 bits | 5 bits | 16 bits |

- (2%) How many registers at most does this computer have?
 - (2%) How many operations at most can this computer have?
 - (2%) What is the range of the number in the Immediate field in 2's complement format?
- (9%) Suppose the execution times for 3 programs on 3 machines are given below:

| | Program X | Program Y | Program Z |
|-----------|-----------|-----------|-----------|
| Machine A | 50 | 30 | 10 |
| Machine B | 10 | 30 | 20 |
| Machine C | 20 | 15 | 10 |

- (3%) Using Program X, Y and Z as benchmarks, please calculate the unweighted arithmetic means of the execution times for the 3 machines.
 - (3%) Using Program X, Y and Z as benchmarks, please calculate the geometric means of the execution times for the 3 machines, with Machine A as the reference machine (as in the SPEC benchmarks).
 - (3%) Which machine has the overall highest performance? Please justify your answer in detail.
- (15%) Suppose we have a direct-mapped cache design with its 32-bit address

| Tag (bit 31-12) | Index (bit 11-4) | Offset (bit 3-0) |
|-----------------|------------------|------------------|
|-----------------|------------------|------------------|

arranged as:

- (2%) What is the cache line size (in words)?
- (2%) How many entries does the cache have?
- (3%) What is the ratio between total bits required for such a cache implementation over the data storage bits?

Starting from power on, suppose the following byte-addressed cache references are recorded: 0, 4, 16, 132, 232, 160, 1024, 30, 140, 3100, 180, 2180.

- (8%) List the final state of the cache, with each valid entry represented as a record of <index, tag, data>.



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[資料結構]

6. [20%] Please explain the following terms

- (a) NP-completeness [4%]
- (b) Binary search trees [4%]
- (c) Minimum spanning trees [4%]
- (d) Hash tables with chaining [4%]
- (e) Huffman code [4%]

7. [10%] Write the *quick-sort* code. Explain its worst case and average case of execution time.8. [10%] What is the *min heap tree*? If these keys (6, 9, 15, 7, 8, 2, 19, 16, 5) are inserted, what is its *min heap tree*?9. [10%] Describe *doubly linked lists* and *singly linked lists*. What are the advantages and disadvantages of doubly linked lists and singly linked lists?