國立台灣科技大學九十九學年度碩士班招生試題

系所組別： 電機工程系碩士班丁組

科　　目： 邏輯設計

（總分為100分）

Problem #1 (10%)

Please do the arithmetic of $(654)_8 - (A3)_{16}$ and convert the result to both BCD and ASCII codes. For the ASCII code, an even parity bit is to be appended at the left.

Decimal	ASCII code	BCD code
0	0110000	0000
1	0110001	0001
2	0110010	0010
3	0110011	0011
4	0110100	0100
5	0110101	0101
6	0110110	0110
7	0110111	0111
8	0111000	1000
9	0111001	1001

Problem #2 (10%)

Please express the Boolean function of F=A+B(C+D) in both sum of minterms and product of maxterms by logic arithmetic.

Problem #3 (15%)

$$F(A,B,C,D) = BC + AB(\overline{C} + D) + AD(\overline{B} + BC) + BC(A + \overline{D}) + B(A\overline{C} + \overline{A}CD)$$

For the above logic expression of *F*, please sketch the Karnaugh map and show the simplest logic expression in both minimum SOP and POS forms.

Problem #4 (10%)

A *PN* flip-flop has four operations, clear to 0, no change, complement, and set to 1, when inputs *P* and *N* are 00, 01, 10, and 11, respectively.

a. Show the characteristic table.

b. Show the characteristic equation.

Problem #5 (20%)

Design a BCD synchronous counter using *JK* flip-flops.

a. Show the state table.

b. **Show all the simplified** flip-flop input equations. (The equations must be in the simplest form.)

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Problem #6 (10%)

Consider a switch-tail ring counter (Johnson counter), where the output from the last flip-flop is inverted and fed back as input to the first flip-flop.

a. Starting from an initial state of 0000, list the sequence of states after each shift until the state returns to 0000.
b. Beginning in the all-0's state (000…0), how many states are there in the count sequence of an n-bit switch-tail ring counter?

Problem #7 (10%)

Obtain the 15-bit Hamming code word for the 11-bit data word 11001001010.

Problem #8 (15%)

An example of the Verilog HDL is shown below.

a. Realize the logic function E with NAND gates.
b. Realize the logic function F with an 8-to-1 multiplexer. Signals A, B, C are connected to the address lines $S_2S_1S_0$ of the multiplexer.
c. Realize the logic function G with a 3-to-8 decoder.

```
// Verilog model: Circuit with Boolean expressions
module Circuit_Boolean_CA(E, F, G, A, B, C, D);
output    E, F, G;
input     A, B, C, D;

assign    E=A|(B&C);
assign    F=A|(B&C)|(~B&D);
assign    G= (~B&C)|(B&~C&~D);
endmodule
```